

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A024A/E	Rev.	1.00
Title	Note on Setting Counter Clock for Independent Watchdog Timer (IWDT) of RX630 Group, RX63N Group, RX631 Group, and RX63T Group		Information Category	Technical Notification		
Applicable Product	RX630 Group RX63N Group RX631 Group RX63T Group	Lot No.	Reference Document	RX630 Group User's Manual: Hardware Rev.1.20 (R01UH0040EJ0120) RX63N Group, RX631 Group User's Manual: Hardware Rev.1.00 (R01UH0041EJ0100) RX63T Group User's Manual: Hardware Rev.1.00 (R01UH0238EJ0100)		
		All				

## 1. Note

When the frequency of the IWDT counter clock is close to the frequency of the peripheral module clock (PCLK), registers associated with the IWDT may not be accessed properly.

## 2. Measure

Set the frequency of the IWDT counter clock to a quarter of the PCLK frequency or lower.

Specifically, set the IWDTCR.CKS[3:0] bits to satisfy the following condition:

$$\text{IWDTCLK} / n \leq \text{PCLK} / 4 \quad (n = 1, 16, 32, 64, 128, 256)$$