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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A867B/E	Rev.	2.00
Title	Note on Procedures for Programming and Erasing the Flash Memory		Information Category	Technical Notification		
Applicable Product	See below.	Lot No. All lots	Reference Document	See below.		

This update concerns usage of the flash memory in the products listed below.

[Precaution]

Processing for a bus master other than the CPU to acquire bus mastership (such as for DMA transfer, DTC transfer, or refreshing the SDRAM) must not proceed during downloading, programming, and erasure.

Otherwise, the downloading, programming, or erasure will not be executed properly.

[Correction of Errors in the Manuals]

Taking the *SH7211 Group Hardware Manual* as an example, we would like to inform you of the correction of errors in the Manuals.

21.5.2 User Program Mode

(2) Programming Procedure in User Program Mode

[Addition (p.926)]

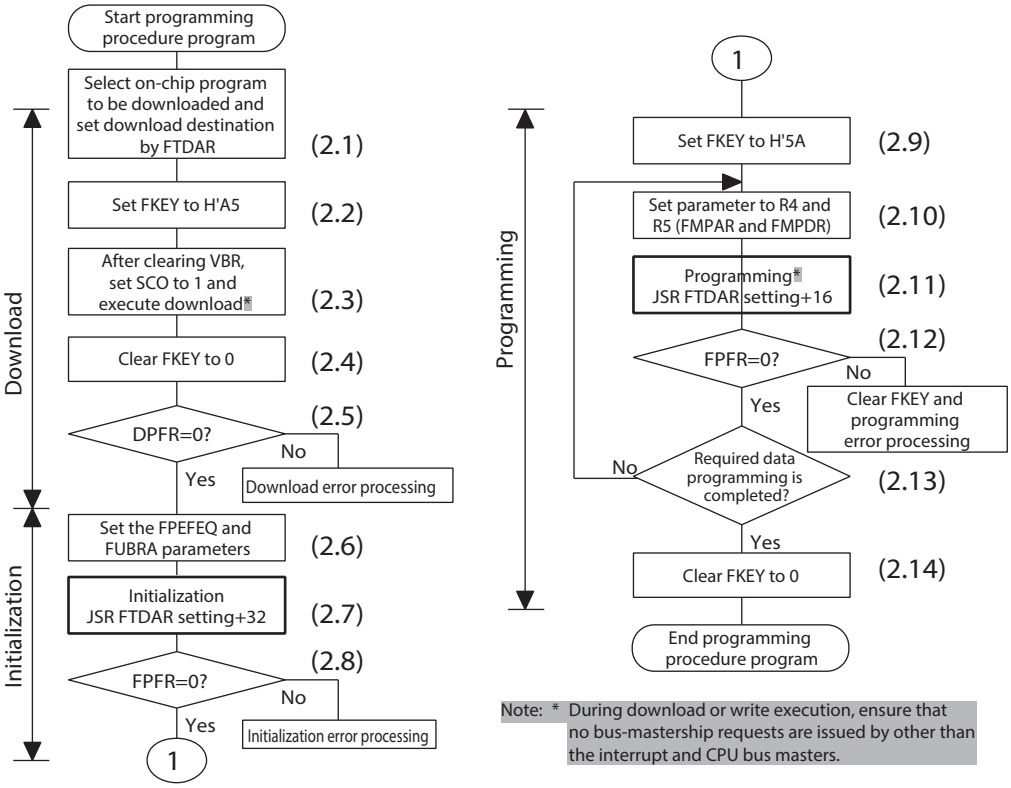

Figure 21.11 Programming Procedure

21.5.2 User Program Mode

(2) Programming Procedure in User Program Mode

[Before correction (p.928)]

1. The user MAT space is switched to the on-chip program storage area.
2. After the selection condition of the download program and the address set in FTDAR are checked, the transfer processing is executed starting to the on-chip RAM address specified by FTDAR.
3. The SCO bits in FCCS, FPCS, and FECS are cleared to 0.
4. The return value is set to the DPFR parameter.
5. After the on-chip program storage area is returned to the user MAT space, execution returns to the user procedure program.

After download is completed and the user procedure program is running, the VBR setting can be changed.

The notes on download are as follows.

In the download processing, the values of the general registers of the CPU are retained.

During the download processing, interrupts must not be generated. For details on the relationship between download and interrupts, see **section 21.7.2, Interrupts during Programming/Erasing**.

Since a stack area of maximum 128 bytes is used, an area of at least 128 bytes must be saved before setting the SCO bit to 1.

If flash memory is accessed by the DMAC or DTC during downloading, operation cannot be guaranteed. Therefore, access by the DMAC or DTC must not be executed.

[After correction]

1. The user MAT space is switched to the on-chip program storage area.
2. After the selection condition of the download program and the address set in FTDAR are checked, the transfer processing is executed starting to the on-chip RAM address specified by FTDAR.
3. The SCO bits in FCCS, FPCS, and FECS are cleared to 0.
4. The return value is set to the DPFR parameter.
5. After the on-chip program storage area is returned to the user MAT space, execution returns to the user procedure program.

After download is completed and the user procedure program is running, the VBR setting can be changed.

The notes on download are as follows.

In the download processing, the values of the general registers of the CPU are retained.

During download processing, ensure that no bus-mastership requests are issued by other than the interrupt and CPU bus masters. For details, see **section 21.7.2, Interrupts during Programming/Erasing**.

Since a stack area of maximum 128 bytes is used, an area of at least 128 bytes must be saved before setting the SCO bit to 1.

21.5.2 User Program Mode

(2) Programming Procedure in User Program Mode

[Addition (p.930)]

(2.11) Programming

There is an entry point of the programming program in the area from (download start address set by FTDAR) + 16 bytes of on-chip RAM.

The subroutine is called and programming is executed by using the following steps.

```
MOV.L  #DLTOP+16,R1         ; Set entry address to R1
JSR    @R1                  ; Call programming routine
NOP
```

1. The general registers other than R0 are saved in the programming program.
2. R0 is a return value of the FPFR parameter.
3. Since the stack area is used in the programming program, a stack area of maximum 128 bytes must be reserved in RAM.
4. During write processing, ensure that no bus-mastership requests are issued by other than the interrupt and CPU bus masters. For details, see **section 21.7.2, Interrupts during Programming/Erasing.**

21.5.2 User Program Mode

(3) Erasing Procedure in User Program Mode

[Addition (p.932)]

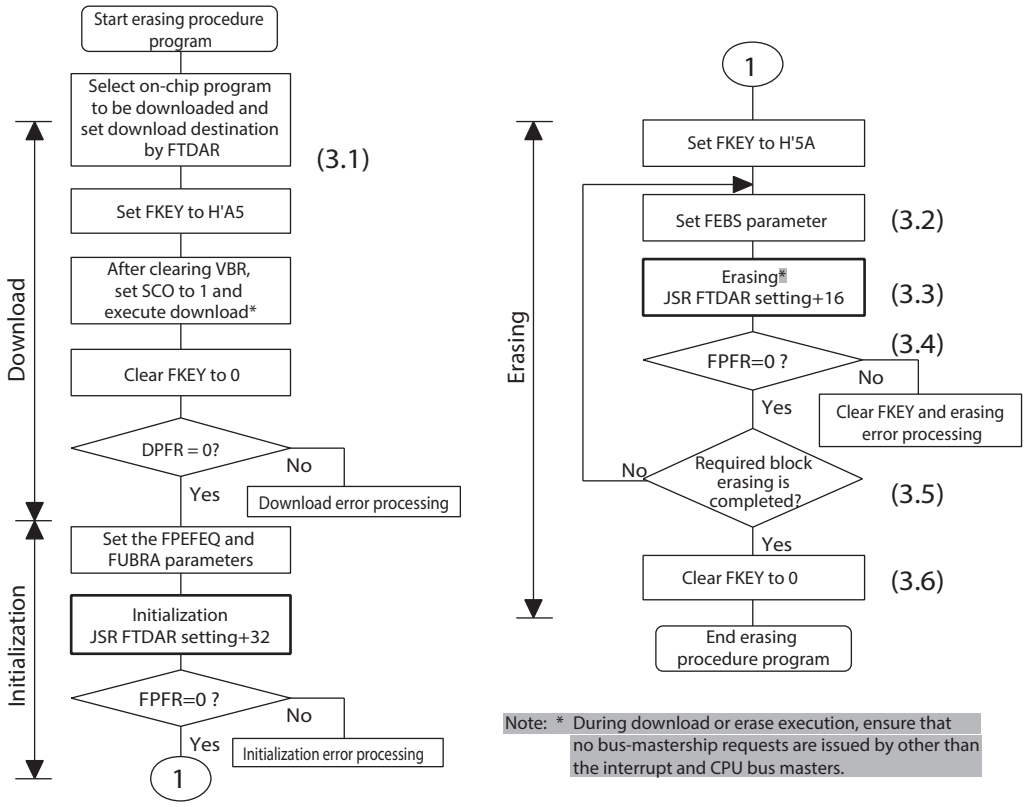

Figure 21.12 Erasing Procedure

21.5.2 User Program Mode

(3) Erasing Procedure in User Program Mode

[Addition (p.933)]

(3.3) Erasure

Similar to as in programming, there is an entry point of the erasing program in the area from (download start address set by FTDAR) + 16 bytes of on-chip RAM. The subroutine is called and erasing is executed by using the following steps.

```
MOV.L  #DLTOP+16,R1        ; Set entry address to R1
JSR    @R1                 ; Call erasing routine
NOP
```

1. The general registers other than R0 are saved in the erasing program.
2. R0 is a return value of the FPFR parameter.
3. Since the stack area is used in the erasing program, a stack area of maximum 128 bytes must be reserved in RAM.
4. During erase processing, ensure that no bus-mastership requests are issued by other than the interrupt and CPU bus masters. For details, see **section 21.7.2, Interrupts during Programming/Erasing**.

21.5.2 User Program Mode

(4) Erasing and Programming Procedure in User Program Mode

[Addition (p.934)]

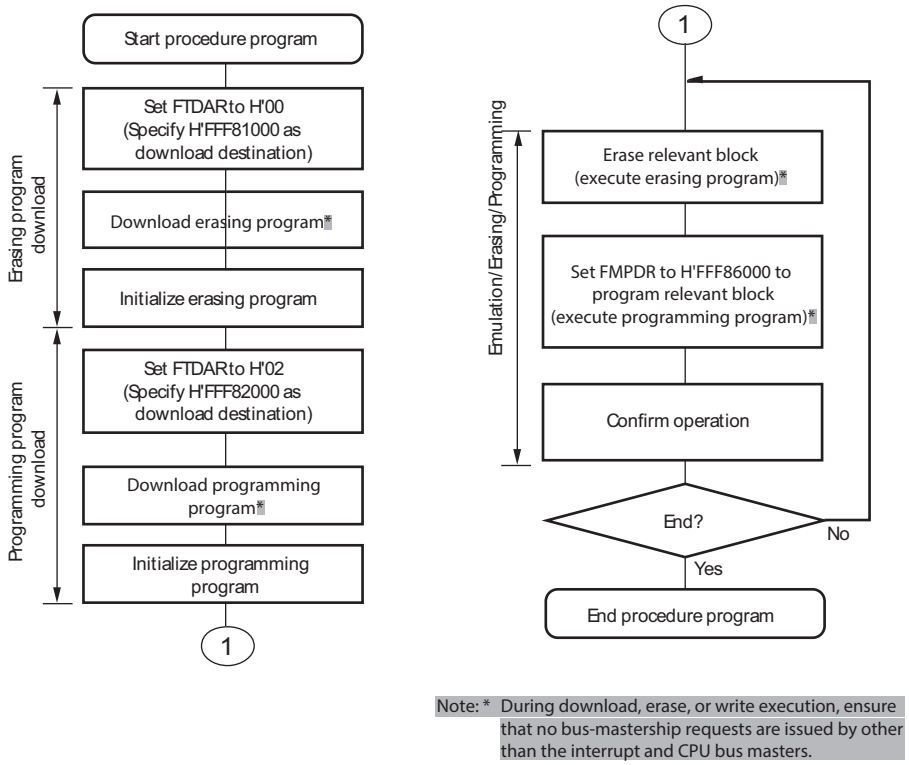

Figure 21.13 Sample Procedure of Repeating RAM Emulation, Erasing, and Programming (Overview)

21.5.3 User Boot Mode

(2) User MAT Programming in User Boot Mode

[Before correction (p.936)]

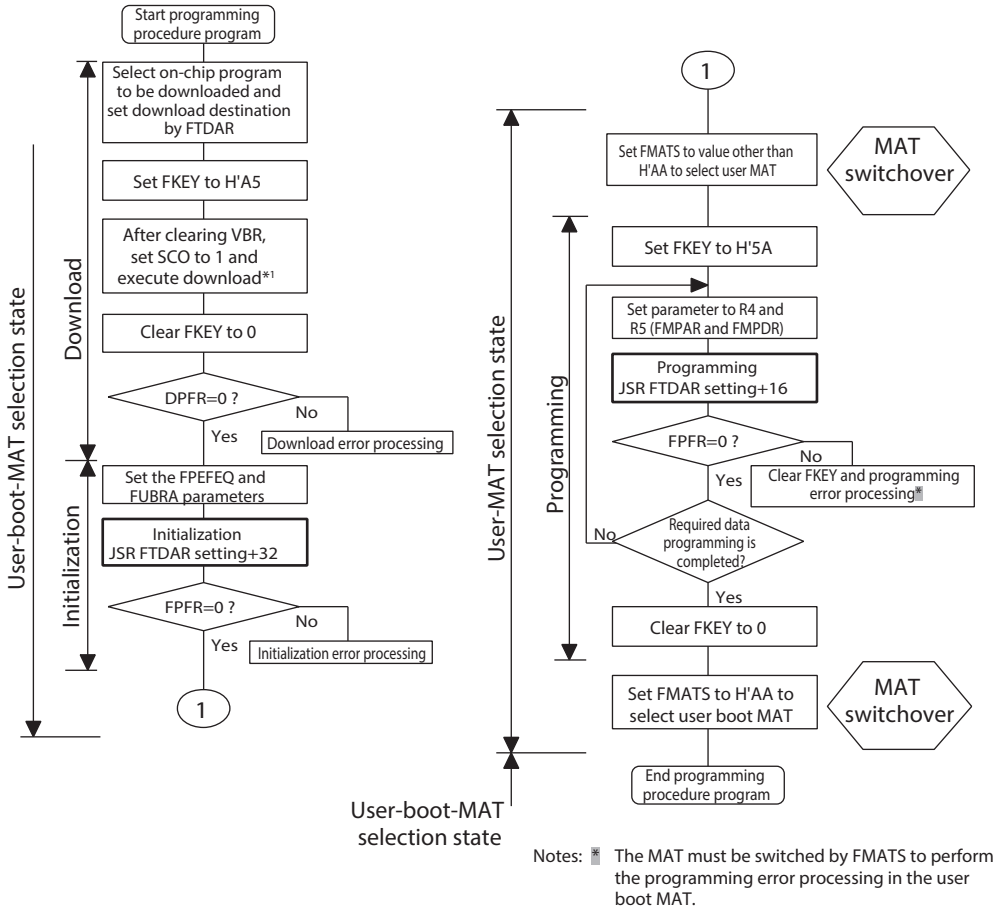

Figure 21.14 Procedure for Programming User MAT in User Boot Mode

[After correction]

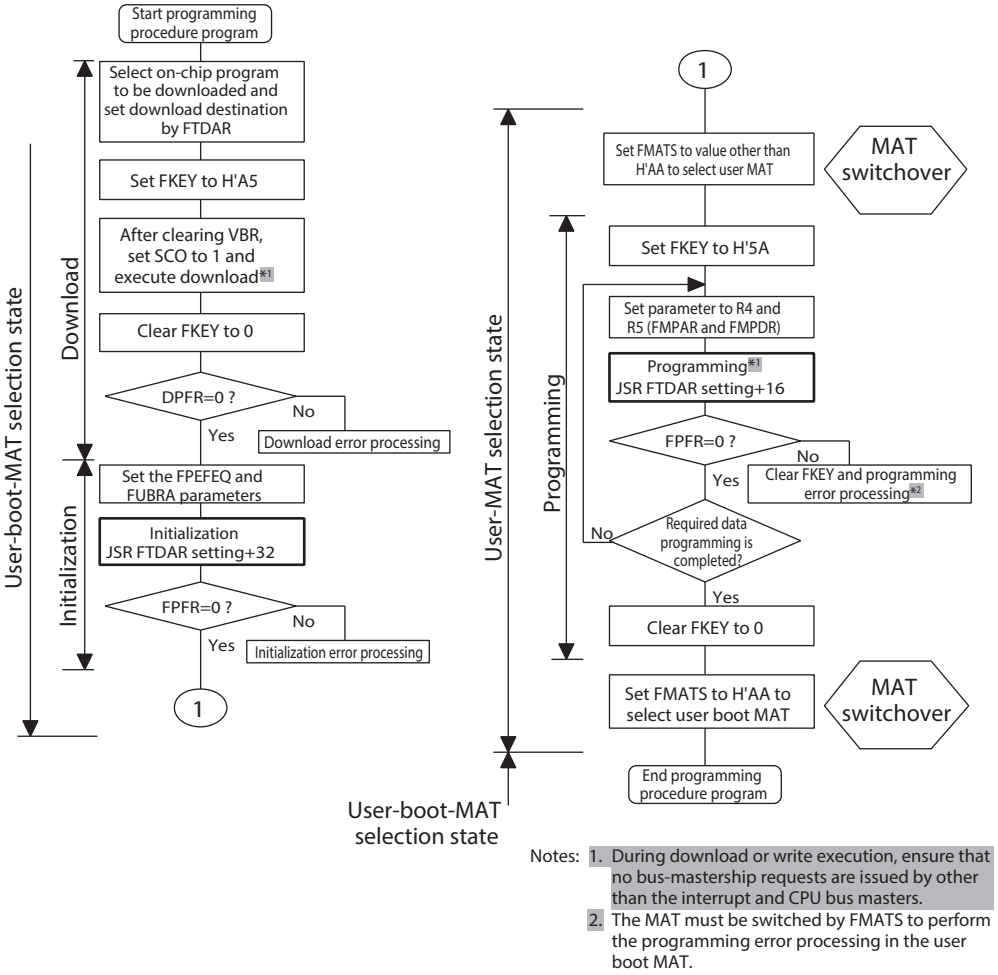

Figure 21.14 Procedure for Programming User MAT in User Boot Mode

21.5.3 User Boot Mode

(3) User MAT Erasing in User Boot Mode

[Before Correction (p.938)]

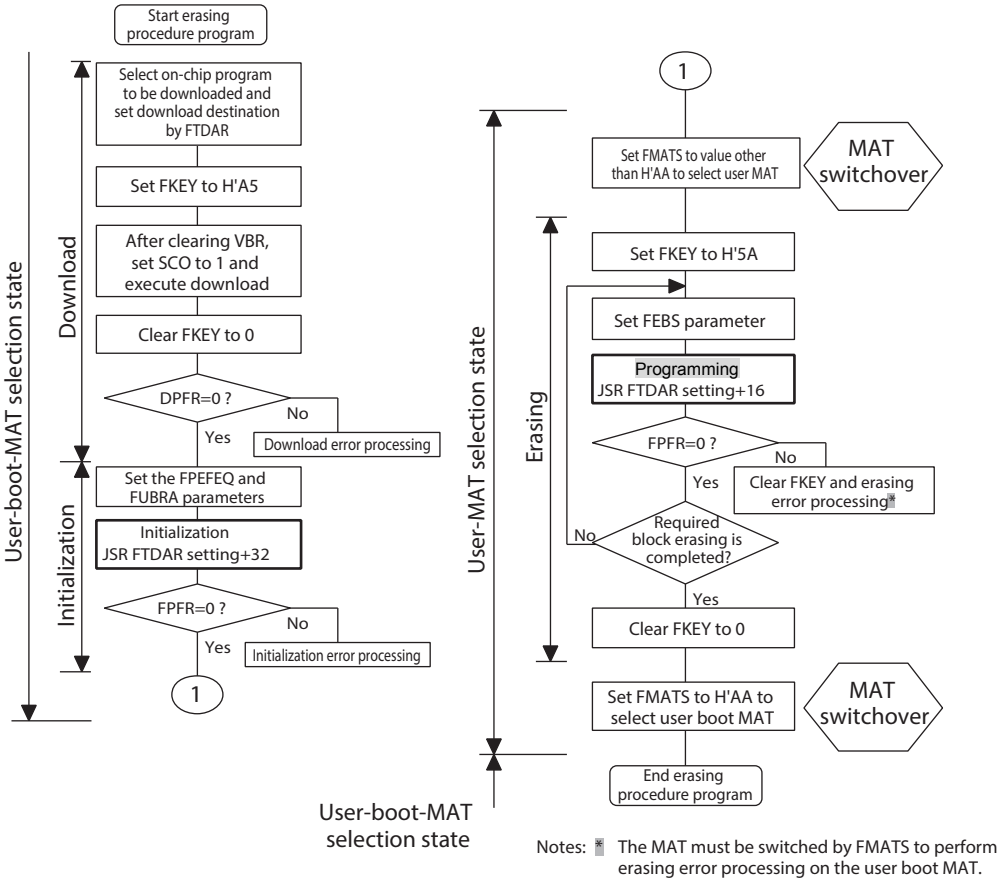

Figure 21.15 Procedure for Erasing User MAT in User Boot Mode

[After correction]

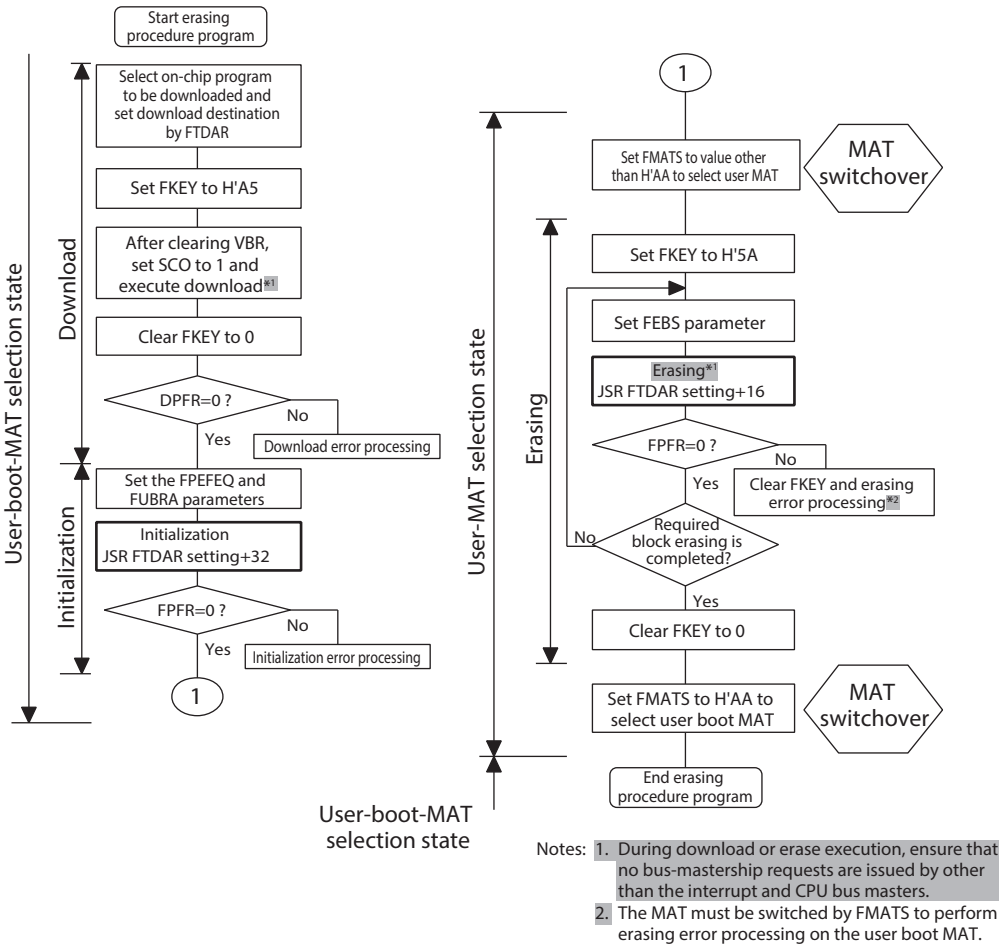

Figure 21.15 Procedure for Erasing User MAT in User Boot Mode

21.7.2 Interrupts during Programming/Erasing

(1) Download of On-Chip Program

[Before Correction (p.944, 945)]

(b) SCO Download Request and Interrupt Request

Download of the on-chip programming/erasing program that is initiated by setting the SCO bit in FCCS to 1 generates a particular interrupt processing accompanied by MAT switchover. Operation when the SCO download request and interrupt request conflicts is described below.

1. Contention between SCO download request and interrupt request

Figure 21.18 shows the timing of contention between execution of the instruction that sets the SCO bit in FCCS to 1 and interrupt acceptance.

2. Generation of interrupt requests during downloading

Ensure that interrupts are not generated during downloading that is initiated by the SCO bit.

[After correction]

(b) SCO Download Request and Interrupt Request

Download of the on-chip programming/erasing program that is initiated by setting the SCO bit in FCCS to 1 generates a particular interrupt processing accompanied by MAT switchover. Operation when the SCO download request and interrupt request conflicts is described below.

1. Contention between SCO download request and interrupt request

   Figure 21.18 shows the timing of contention between execution of the instruction that sets the SCO bit in FCCS to 1 and interrupt acceptance.

2. Generation of interrupt requests during downloading

   Securing of bus-mastership by other than the interrupt and CPU bus masters (DMA transfer, DTC transfer, SDRAM refresh) is prohibited during SCO download execution.

21.7.2 Interrupts during Programming/Erasing

(2) Interrupts during Programming/Erasing

[Before correction (p.946)]

Ensure that NMI, IRQ, and all other interrupts are not generated during programming or erasing of on-chip program code.

[After correction]

Securing of bus-mastership by other than the interrupt and CPU bus masters (DMA transfer, DTC transfer, SDRAM refresh) is prohibited during programming or erase execution by a downloaded on-chip program.

[Applicable Products and Related Documents]

Family	Group	Related Documents	Rev.	Control Code
SH7080	SH7083, SH7084, SH7085, SH7086	SH7080 Group User's Manual: Hardware	5.00	R01UH0198EJ0500
SH7137	SH7131, SH7132, SH7136, SH7137	SH7137 Group Hardware Manual	3.00	REJ09B0402-0300
SH7146	SH7146, SH7149	SH7146 Group User's Manual: Hardware	4.00	R01UH0049EJ0400
SH7210	SH7211	SH7211 Group Hardware Manual	3.00	REJ09B0344-0300
SH7243	SH7243	SH7280 Group, SH7243 Group User's Manual: Hardware	3.00	R01UH0229EJ0300
SH7280	SH7285, SH7286	SH7280 Group, SH7243 Group User's Manual: Hardware	3.00	R01UH0229EJ0300