This document is a cautionary note regarding IO0FV[1:0] bits in the Common Control Register (CMNCR) of the SPI Multi I/O Bus Controller in products of the RZ/A2M Groups.

### Description of the IO0FV[1:0] bits

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9, 8</td>
<td>IO0FV[1:0]</td>
<td>11</td>
<td>R/W</td>
<td>QSPIn.IO0 Fixed Value for 1-bit Size</td>
</tr>
</tbody>
</table>

Fixes the output value of QSPIn.IO0 pin for 1-bit size.

- 00: The output value is 0.
- 01: The output value is 1.
- 10: The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer).
- 11: The pin is placed in the Hi-Z state.

Note. Set these bits to 11 (the pin is placed in the Hi-Z state) when data read transfer size is not 1-bit.