This document is a cautionary note regarding HS bit in the PHY Control Register (PHYCNT) of the SPI Multi I/O Bus Controller in products of the RZ/A2M Groups.

**[Description of the HS bit]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>HS</td>
<td>0</td>
<td>R/W</td>
<td>High-Speed Response Mode</td>
</tr>
</tbody>
</table>

- Specifies the high-speed response mode.
- 0: Data is read for the number of data units specified in the RBURST bits of the DCR register and then output to the bus master.
- 1: The read data is output to bus master in parallel of device access when DCR.RBE = 1.

**Note 1.** When this bit is set to 1, use DMA transfer. The transfer size in the RBURST[4:0] bits of the DCR register should be fixed to 5'h1F.

**Note 2.** Do not access the register area during DMA transfer.

**Note 3.** When this bit is set to 1, access address alignment to SPI multi I/O bus space should be 256Byte align and clear the cache entry by setting the RCF bit in DCR to 1 before starting DMA transfer.