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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0066A/E	Rev.	1.00
Title	Note on HS bit of the SPI Multi I/O Bus Controller of RZ/A2M Group Products		Information Category	Technical Notification		
Applicable Product	RZ/A2M Group	Lot No. All	Reference Document	RZ/A2M Group User's Manual: Hardware Rev.3.00 (R01UH0746EJ0300)		

This document is a cautionary note regarding HS bit in the PHY Control Register (PHYCNT) of the SPI Multi I/O Bus Controller in products of the RZ/A2M Groups.

[Description of the HS bit]

Bit	Bit Name	Initial Value	R/W	Description
18	HS	0	R/W	High-Speed Response Mode Specifies the high-speed response mode. 0 : Data is read for the number of data units specified in the RBURST bits of the DRCR register and then output to the bus master. 1 : The read data is output to bus master in parallel of device access when DRCR.RBE = 1. Note 1. When this bit is set to 1, use DMA transfer. The transfer size in the RBURST[4:0] bits of the DRCR register should be fixed to 5'h1F. Note 2. Do not access the register area during DMA transfer. Note 3. When this bit is set to 1, access address alignment to SPI multi I/O bus space should be 256Byte align and clear the cache entry by setting the RCF bit in DRCR to 1 before starting DMA transfer.