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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-V85-A006A/E	Rev.	1.00
Title	Note about the RYO output delay time of the clock synchronous serial interface (CSIH, CSIG)		Information Category	Technical Notification		
Applicable Product	V850E2/Px4 series V850E2/Px4-L series	Lot No. All lots	Reference Document	User Manual of each product		

There is modification in an electrical characteristic of clock synchronous serial interface (CSIH, CSIG) RYO output delay.

This RENESAS Technical update will mention the change contents and the manual correction contents.

1. Modification items

The target function blocks (CSIH, CSIG) of each product series are shown in table below.

Product nick name	Spec change function block
V850E2/Px4	CSIG, CSIH
V850E2/Px4-L	CSIG

(1) Electrical characteristic change at the CSIG slave mode (RYO output delay).

When CSIGnSC cycle time (tKCYS) is smaller than 8 times of the PCLK cycle (tPCLK) as following figure 1,

1 cycle tPCLK is added to the RYO output delay (tSRYO).

There is no spec change when CSIGnSC cycle time (tKCYS) is more than 8 times PCLK cycle.

(2) Electrical characteristic change at the CSIH slave mode (RYO output delay).

When CSIHnSC cycle time (tKCYS) is smaller than 8 times of the PCLK cycle (tPCLK) as following figure 1,

1 cycle tPCLK is added to the RYO output delay (tSRYO).

There is no spec change when CSIHnSC cycle time (tKCYS) is more than 8 times PCLK cycle.

Note:
Refer to User Manual of each product for details of the register and its setting.

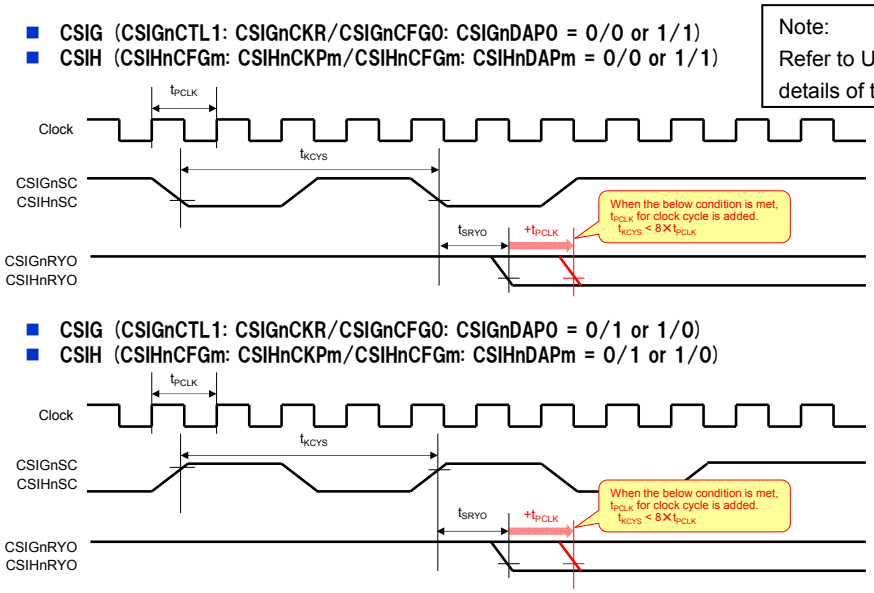

Figure 1. CSIGnSC/CSIHnSC and CSIGnRYO/CSIHnRYO timing chart

2. Manual modification

2-1. V850E2/Px4

(1) CSIG Electrical characteristic modification points

The CSIGnRYO output delay (tSRYO) is changed as below.

Item	Symbol	Conditions	MIN.	TYP.	MAX.	unit
CSIGnRYO output delay	t_{SRYO}	tKCYS ≧ 8×tPCLK			30	ns
		tKCYS ＜ 8×tPCLK			30 + t_{PCLK}	ns

(2) CSIH Electrical characteristic modification points

The CSIHnRYO output delay (tSRYO) is changed as below.

Item	Symbol	Condition	MIN.	TYP.	MAX.	unit
CSIHnRYO outout delay	t_{SRYO}	tKCYS ≧ 8×tPCLK			30	ns
		tKCYS ＜ 8×tPCLK			30 + t_{PCLK}	ns

2-2. V850E2/Px4-L

(1) CSIG Electrical characteristic modification points

The CSIGnRYO output delay (tSRYO) is changed as below.

Item	Symbol	Condition	MIN.	TYP.	MAX.	unit
CSIGnRYO output delay	t_{SRYO}	tKCYS ≧ 8×tPCLK			30	ns
		tKCYS ＜ 8×tPCLK			30 + t_{PCLK}	ns