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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-V85-A014A/E	Rev.	1.00
Title	Note about the RYO output delay time of the clock synchronous serial interface (CSIH)		Information Category	Technical Notification		
Applicable Product	V850E2/Sx4-H series	Lot No. All lots	Reference Document	Data Sheet of each product		

There is modification in an electrical characteristic of clock synchronous serial interface (CSIH) RYO output delay.

This RENESAS Technical update will mention the change contents and the manual correction contents.

1. Modification items

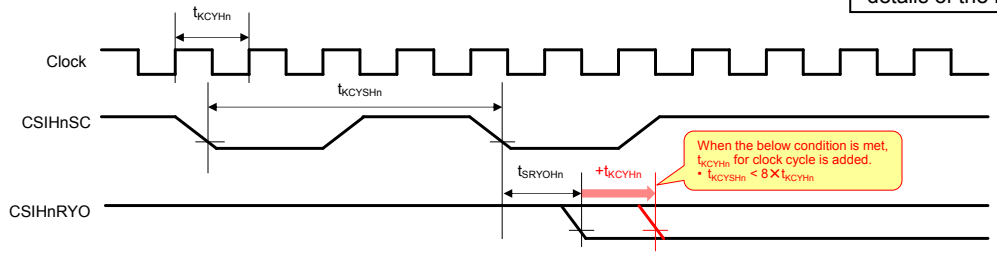
(1) Electrical characteristic change at the CSIH slave mode (RYO output delay).

When CSIHnSC cycle time (tKCYSHn) is smaller than 8 times of the Macro Operation clock cycle time (tKCYHn) as following figure 1, 1 cycle tKCYHn is added to the RYO output delay (tSRYOHn).

There is no spec change when CSIHnSC cycle time (tKCYSHn) is more than 8 times of the Macro Operation clock cycle time.

Note:
Refer to User Manual of each product for details of the register and its setting.

■ CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



■ CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/1 or 1/0)

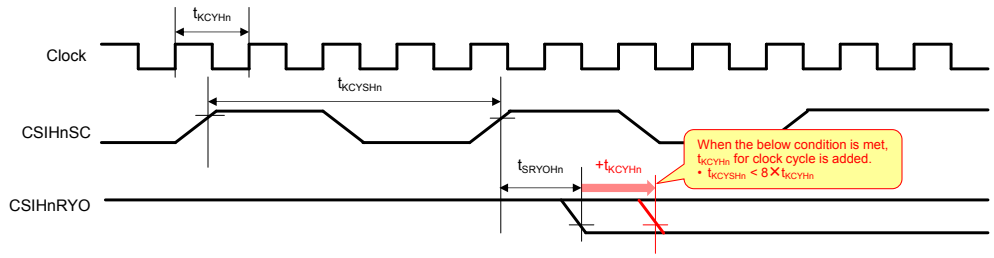


Figure 1. CSIHnSC and CSIHnRYO timing chart

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2. Manual modification

(1) CSIH Electrical characteristic modification points

The CSIHnRYO output delay (tSRYOHn) is changed as below.

Item	Symbol	Condition	MIN.	TYP.	MAX.	unit
CSIHnRYO outout delay	t_{SRYOHn}	tKCYSHn ≧ 8×tKCYHn			30	ns
		tKCYSHn ＜ 8×tKCYHn			30 + t_{KCYHn}	ns