RENESAS TECHNICAL UPDATE

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Note about the RY output delay time of the cl synchronous serial interface (CSIG)	Information Category	Technical Notification									
V850E2/Dx4 series Lot No. V850E2/Dx4-H series All lots Reference Data Sheet of each product											
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CSIGnSC cycle time (tKCYS) is smaller than 8 tKCY is added to the CSIG0RY output delay times the the compared to the the compared to the	times of the ne (tDRYO)	Module clock cy	cle time (tKCY) as follo		re 1,						
 CSIG (CSIGOCFGO.CSIGOCKP / CSIGnCTL1.CSIGnCKR = 0/0 or 1/1) Clock											
CSIGORYO Figure 1. CSIGOSC and CSIGORY timing chart											
	Note about the RY output delay time of the cl synchronous serial interface (CSIG) V850E2/Dx4 series V850E2/Dx4-H series iffication in an electrical characteristic of clock s AS Technical update will mention the change c ion items cal characteristic change at the CSIG slave mod CSIGnSC cycle time (tKCYS) is smaller than 8 the tKCY is added to the CSIG0RY output delay times in o spec change when CSIGnSC cycle time (the CSIG (CSIGOCFGO.CSIGOCKP / CSIGnCTL1.0 Clock the GOSC the clock t	Note about the RY output delay time of the clock synchronous serial interface (CSIG) V850E2/Dx4 series V850E2/Dx4-H series All lots dification in an electrical characteristic of clock synchronous AS Technical update will mention the change contents and ion items cal characteristic change at the CSIG slave mode (CSIG0R CSIGnSC cycle time (tKCYS) is smaller than 8 times of the tKCY is added to the CSIG0RY output delay time (tDRYO) is no spec change when CSIGnSC cycle time (tKCYS) is m CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock Corro CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock Corro CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock CORYO CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = Clock	No. Note about the RY output delay time of the clock synchronous serial interface (CSIG) V850E2/Dx4 series V850E2/Dx4 series V850E2/Dx4-H series Lot No. All lots Reference Document diffication in an electrical characteristic of clock synchronous serial interface AS Technical update will mention the change contents and the manual corr ion items all characteristic change at the CSIG slave mode (CSIG0RY output delay to CSIGNSC cycle time (tKCYS) is smaller than 8 times of the Module clock cy tKCY is added to the CSIG0RY output delay time (tDRYO). s no spec change when CSIGNSC cycle time (tKCYS) is more than 8 times CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = 0/0 or 1/1) clock terro terro CSIG (CSIG0CFG0.CSIG0CKP / CSIGnCTL1.CSIGnCKR = 0/1 or 1/0) clock terro	No. IN-V83-A029A/E No. IN-V85-A029A/E No. IN-V85-A029A/E Note: Note: Reference Data Sheet of each pro- Note: Reference Note: Refere	No. IN-V85-AU25A/E Ref. Note about the RY output delay time of the clock synchronous serial interface (CSIG) Information Category Technical Notification V850E2/Dx4 series V850E2/Dx4-H series Lot No. Reference Document Data Sheet of each product uiffication in an electrical characteristic of clock synchronous serial interface (CSIG) CSIGORY output delay ti AS Technical update will mention the change contents and the manual correction contents. Information interms al characteristic change at the CSIG slave mode (CSIGORY output delay time). SIGnSC cycle time (tKCY) is smaller than 8 times of the Module clock cycle time (tKCY) as following figur tKCY is added to the CSIGORY output delay time (tDRYO). s no spec change when CSIGNCKP / CSIGNCTL1.CSIGNCKR = 0/0 or 1/1) Note: Refer to User Manual of each prod details of the register and its settin tore there detains of the Module clock cycle time. CSIG (CSIGOCFG0.CSIGOCKP / CSIGNCTL1.CSIGNCKR = 0/1 or 1/0) Information there detains of the content and						



2. Manual modification

(1) CSIG Electrical characteristic modification points

The CSIG0RY output delay time (tDRYO) is changed as below.

Parameter	СТ	Symbol	Condition		Ratings			Unit
					MIN.	TYP.	MAX.	
Ready / Busy output signal (CSIG0RY)	DS	tDRYO	filtered (DNF) ^a	$tKCYS \ge 8 \times tKCY$			30 + tdDNFSCI(max)	ns
output delay time (vs. CSIG0SC input) ^d				tKCYS < 8×tKCY			30 + tdDNFSCI(max) + tKCY	ns
			filter-bypassed ^c	tKCYS ≧ 8×tKCY			30	ns
				tKCYS < 8×tKCY			30+tKCY	ns

