To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	Microprocessor			No	TN-SH7-463A/E	Rev	1
THEME	Modification of the SH7705 Hardware Manual about DMAC		Classification of Information	1. Spec change (2) Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	HD6417705	Lot No. ALL	Reference Documents	SH7705 Hardware Manual Rev.1.0 ADE-602-276		Effective Date Eternity	

There is a correction of SH7705 Hardware Manual about DMAC.

page 312, Bus Mode and Channel Priority

[before modification]

When a given channel 1 is transferring in burst mode and there is transfer request to channel 0 with a high priority, the transfer of channel 0 will begin immediately.

At this time, if the priority is set in fixed mode (CH0>CH1), the channel 1 transfer will continue when the channel 0 transfer has completely finished, even if channel 0 is operating in cycle steal mode or in burst mode.

If the priority is set in round-robin mode, channel 1 will begin operating again after channel 0 completes the transfer of one transfer unit, even if channel 0 is in cycle steal mode or in burst mode. The bus mastership will then switch between the two in the order channel 1, channel 0, channel 1, channel 0.

Even if the priority is set in fixed mode or in round-robin mode, it will not give the bus mastership to the CPU since channel 1 is in burst mode. This example is illustrated in figure 8.12.

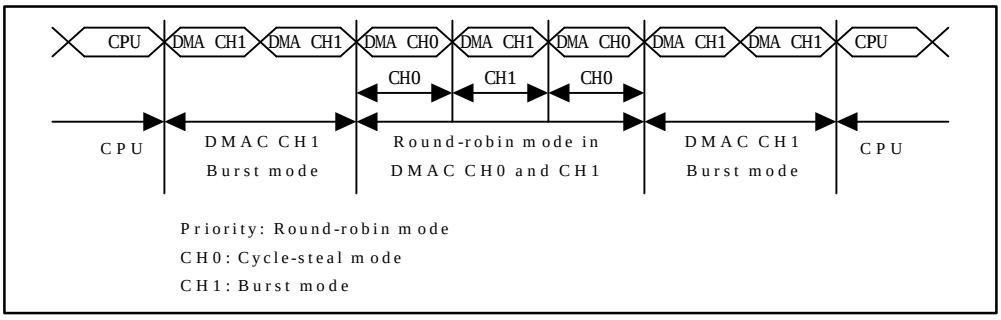

Figure 8.12 Bus State when Multiple Channels are Operating

[after modification]

If the priority is set in fixed mode (CH0>CH1), when a given channel 1 is transferring in burst mode and there is a transfer request to a channel 0 with a higher priority, the transfer of channel 0 will begin immediately.

At this time, if the channel 0 is set in burst mode, the channel 1 transfer will continue when the channel 0 transfer has completely finished.

If the channel 0 is set in cycle steal mode, channel 1 will begin operation again after channel 0 completes the transfer of one transfer unit without giving the internal bus mastership to CPU. The bus mastership will then switch between the two in the order channel 0, channel 1, channel 0, channel 1. In other words, the burst transfer steals the CPU cycle after the cycle steal transfer. This example is illustrated in figure 8.12. If there are several channels set to burst mode, the top priority channel will execute the transfer.

When DMA transfer operates in several channels, the bus mastership will not be given to other bus-masters until all the burst transfer has completed.

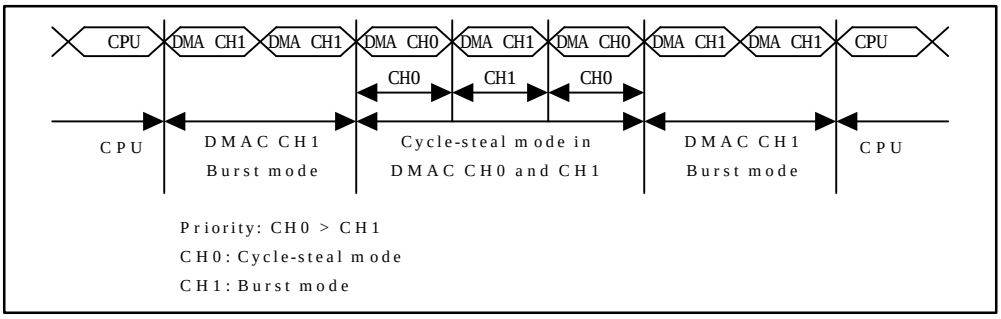

Figure 8.12 Bus State when Multiple Channels are Operating

In round-robin mode, the priority order changes as shown in Fig.8.4. But the channel in the cycle steal mode and the channel in the burst mode cannot be used simultaneously.