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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-V85-A035A/E	Rev.	1.00
Title	Misdescription in the electrical characteristics of the bus timing		Information Category	Technical Notification		
Applicable Product	V850ES/FJ3, V850ES/FJ3-N series V850ES/FK3, V850ES/FK3-N series	Lot No. All lots	Reference Document	Data Sheet & User Manual : Hardware of applicable products		

In the Data Sheet & User Manual: Hardware of the Applicable Products which indicated in “Applicable Product“, the electrical characteristics of the bus timing is corrected as follows.

1. Notification1 Data Sheet

The bus timing of “Address output time from _RD↑” and “Delay time from _RD↑ to ASTB↓” are changed as below.

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2. Electrical Specifications of (A)-Grade

2.7 AC Characteristics

2.7.2 Bus Timing (Multiplexed bus mode)

(a) CLKOUT asynchronous: In multiplexed bus mode

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V,

VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Before correction:

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Address output time from _RD↑	tDRDA	<21>		(1+i+tAHW)T-15		ns
Delay time from _RD↑ to ASTB↓	tDRDST	<23>		(1.5+i+tAHW)T-15		ns

After correction:

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Address output time from _RD↑	tDRDA	<21>		(1+i+t)T-15		ns
Delay time from _RD↑ to ASTB↓	tDRDST	<23>		(1.5+i+tASW)T-15		ns

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Current datasheet is saying that TI state (Idle state) of TAHW state (Address hold wait state) would be existed between the read cycle. But in actually, there isn’t the TAHW state between read cycle.

If customer’s system does not set TAHW state, there is no impact.

Or, if TAHW state is set and TAHW state between read cycle is supposed, there could be some influence.

Therefore, please reconfirm your system’s condition.

2. Notification2 User Manual

The figure of “Timing: write data with address setup/hold wait (bus size: 16-bit)” is changed as below.

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Chapter 9. Bus and Memory Control (BCU, MEMC)

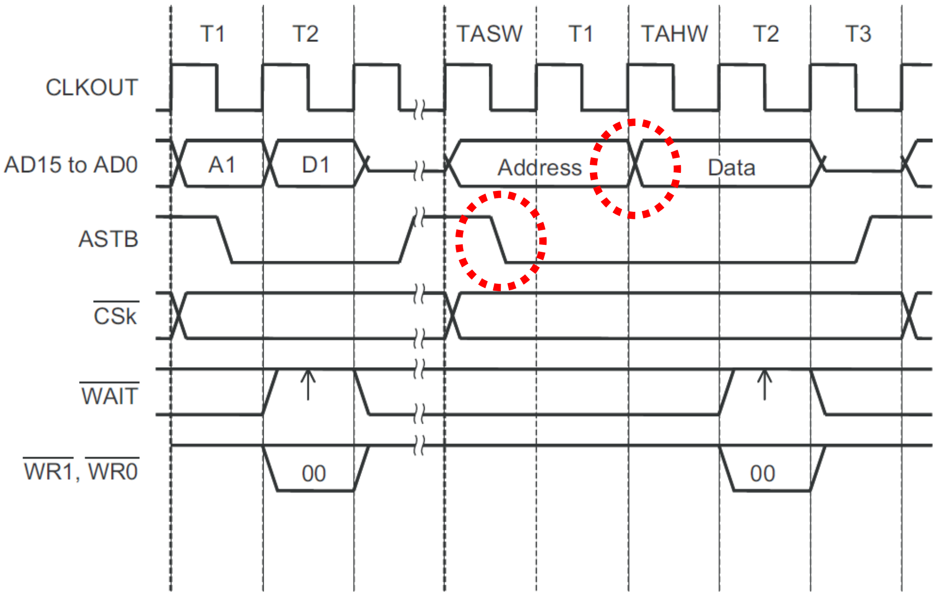
9.5 External Devices Interface Timing

9.5.1 Writing to external devices

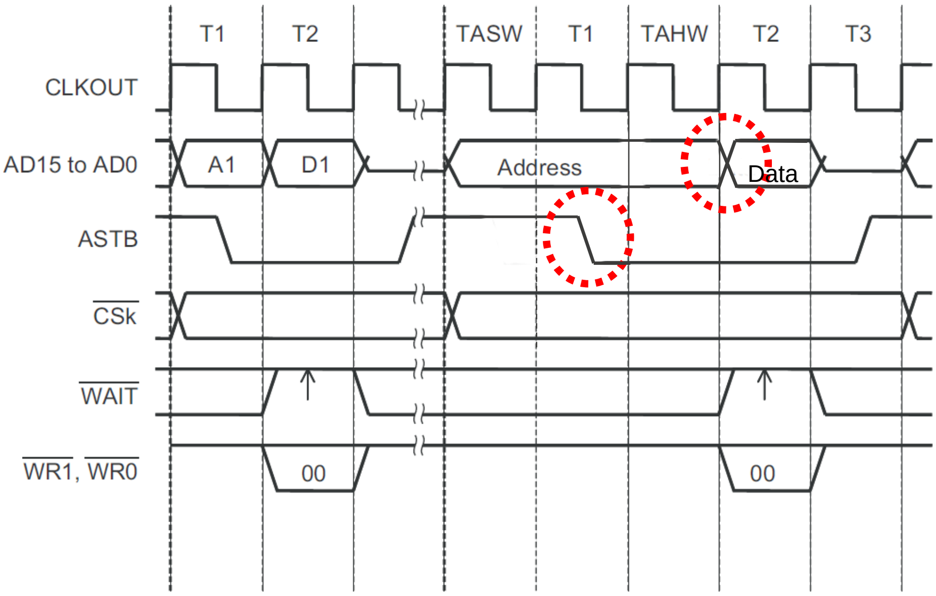
(3) Write with address setup/hold wait (bus size: 16-bit)

Figure 9-9 Timing: write data with address setup/hold wait (bus size: 16-bit)

Before correction:



After correction:



3. Applicable Products

V850ES/FJ3

- μ PD70F3378
- μ PD70F3379
- μ PD70F3380
- μ PD70F3381
- μ PD70F3382

V850ES/FK3

- μ PD70F3383
- μ PD70F3384
- μ PD70F3385

V850ES/FJ3-N

- μ PD70F3631
- μ PD70F3632
- μ PD70F3633
- μ PD70F3634
- μ PD70F3635

V850ES/FK3-N

- μ PD70F3636
- μ PD70F3637
- μ PD70F3638