

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-16C-A163A/E	Rev.	1.00
Title	M32C/87 Group Document Revision for UART5 and UART6 in Serial interfaces (Serial I/O)		Information Category	Technical Notification		
Applicable Product	M32C/87 Group	Lot No.	Reference Document			

The description of the UiC0 register (UARTi Transmit/Receive Control Register 0) (i = 0 to 6) has been revised. When using the subject documents, please pay attention to the changes.

1. Subject Documents

M32C/87 Group Hardware Manual Rev.0.20
M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual Rev.1.00

2. Corrections

Refer to the following page in the subject documents.

M32C/87 Group Hardware Manual Rev.0.20
Page 196 (Figure 16.7) U0C0 to U6C0 registers

M32C/87 Group (M32C/87, M32C/87A, M32C/87B) Hardware Manual Rev.1.00
Page 200 (Figure 17.7) U0C0 to U6C0 registers

Rev.1.00 is used as an example for corrections shown in the following pages.

UiC0 register (UARTi Transmit/Receive Control Register 0) (i = 0 to 6) (Before)

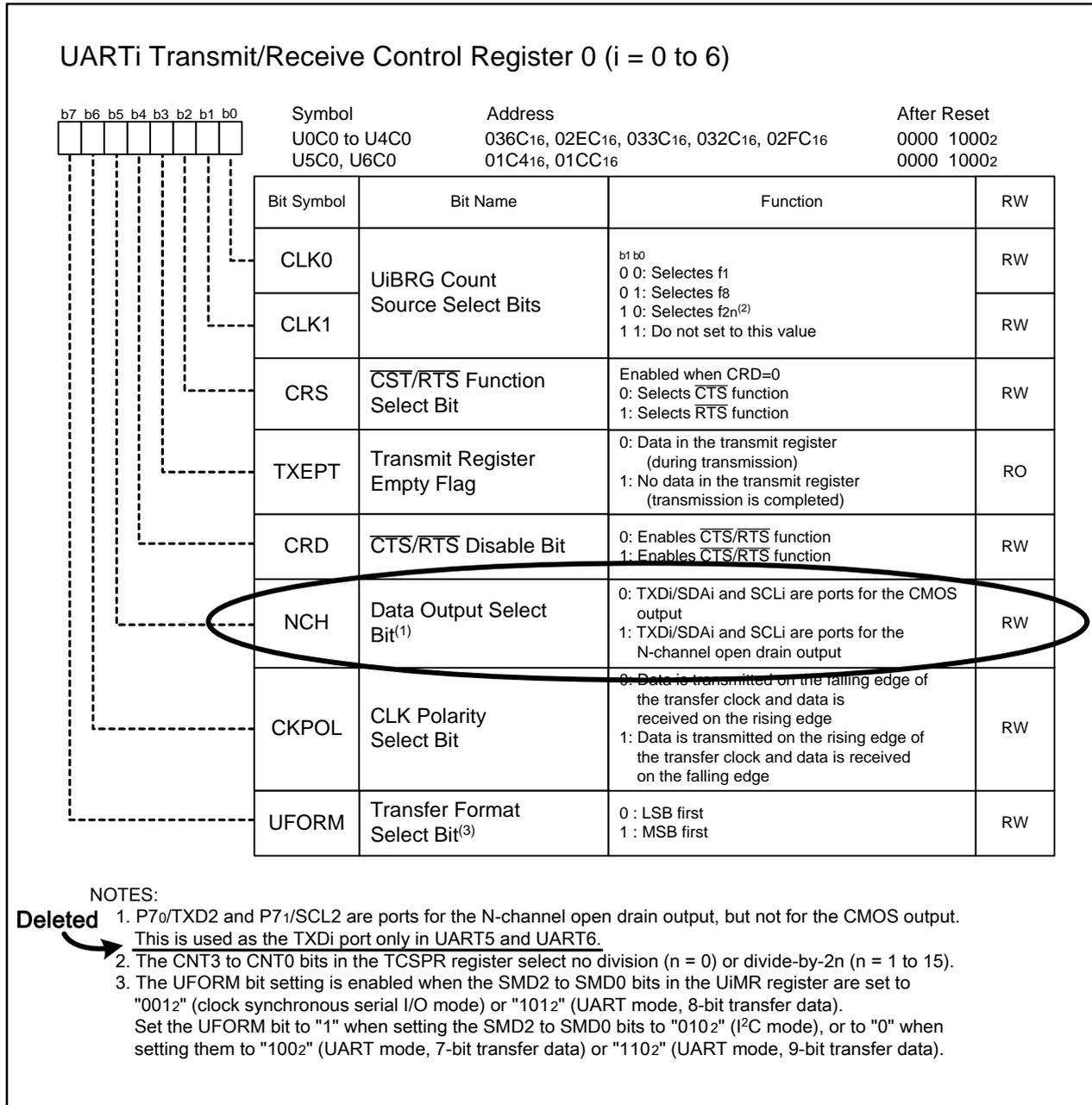
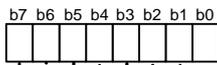


Figure 17.7 U0C0 to U6C0 Registers

UiC0 register (UARTi Transmit/Receive Control Register 0) (i = 0 to 6) (After)

UARTi Transmit/Receive Control Register 0 (i = 0 to 6)



Symbol	Address	After Reset
U0C0 to U4C0	036C ₁₆ , 02EC ₁₆ , 033C ₁₆ , 032C ₁₆ , 02FC ₁₆	0000 1000 ₂
U5C0, U6C0	01C4 ₁₆ , 01CC ₁₆	0000 1000 ₂

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG Count Source Select Bit	b1 b0 0 0: Selectes f1 0 1: Selectes f8 1 0: Selectes f2n ⁽²⁾ 1 1: Do not set to this value	RW
CLK1			RW
CRS	CTS/RTS Function Select Bit	Enabled when CRD=0 0: Selects CTS function 1: Selects RTS function	RW
TXEPT	Transmit Register Empty Flag	0: Data in the transmit register (during transmission) 1: No data in the transmit register (transmission is completed)	RO
CRD	CTS/RTS Disable Bit	0: Enables CTS/RTS function 1: Enables CTS/RTS function	RW
NCH	Data Output Select Bit ⁽¹⁾⁽⁴⁾	0: TXDi/SDAi and SCLi are ports for the CMOS output 1: TXDi/SDAi and SCLi are ports for the N-channel open drain output	RW
CKPOL	CLK Polarity Select Bit	0: Data is transmitted on the falling edge of the transfer clock and data is received on the rising edge 1: Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge	RW
UFORM	Transfer Format Select Bit ⁽³⁾	0: LSB first 1: MSB first	RW

NOTES:

- P7₀/TXD₂ and P7₁/SCL₂ are ports for the N-channel open drain output, but not for the CMOS output.
- The CNT₃ to CNT₀ bits in the TCSPR register select no division (n = 0) or divide by 2ⁿ (n = 1 to 15).
- The UFORM bit setting is enabled when the SMD₂ to SMD₀ bits in the UiMR register are set to "001₂" (clock synchronous serial I/O mode) or "101₂" (UART mode, 8-bit transfer data). Set the UFORM bit to "1" when setting the SMD₂ to SMD₀ bits to "010₂" (I²C mode), or to "0" when setting them to "100₂" (UART mode, 7-bit transfer data) or "110₂" (UART mode, 9-bit transfer data).
- This bit is reserved in UART5 and UART6. Set to "0".

Figure 17.7 U0C0 to U6C0 Registers