To our customers,

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GRADE A

RENESAS TECHNICAL NEWS

No.M16C-112-0309

M30245MC/8-XXXGP

Cautions on Serial I/O

Classification	Concerned Products
Corrections and supplementary explanation of document ö Notes Knowhow Others	M30245MC/8-XXXGP Note: The cautions and description of the behavior are not applied to M30245FCGP.

1. Cautions

Under the condition below, there is a possibility that the cycle when the first data transfer is available is delayed for 256 cycles (maximum) of BRG count source.

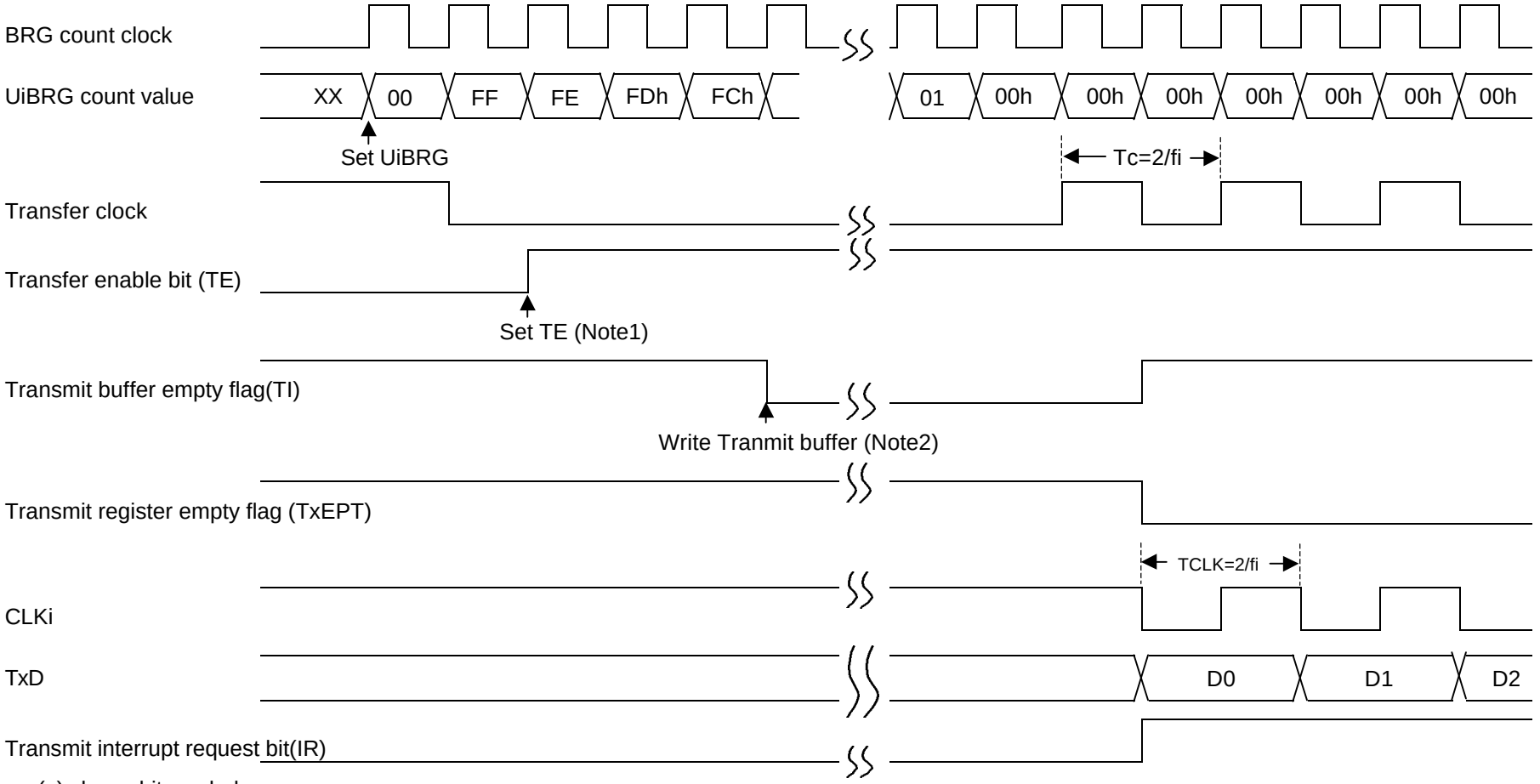
- UiBRG= 00h (no division)
- Clock synchronous serial I/O mode (internal clock or external clock)
- UART mode (internal clock)

Due to the delay of the cycle when the first data transfer is available, Transmit register empty flag (TXEPT) is delayed as well. Please consider the delay when judging TXEPT to know the status of the transfer.

2. Description of the behavior

BRGi divides the count source by n+1 (n: value set to UiBRG). The divide-by-two signal of the underflow signal is UARTi Transfer clock or UARTi Receive clock. In case that UiBRG is set to ‘00h’, there is a possibility that the first underflow of BRG is delayed for 256 cycles. Therefore, data transfer is not available until the first underflow is generated. Underflows except the first time are generated during the expected cycle (no division). The timing diagram in the next page shows an example of the behavior.

Operation when UiBRG is set to '00h'



( ) shows bit symbol

The timing diagram is under the condition below.
- Clock synchronous serial I/O mode
- internal clock
- CLK polarity select bit = '0'
- Transmit interrupt cause select bit = '0'
- BRG ='00h'

Note1: Timing when TE is set depends on operation code.
Note2: Timing when TI is cleared depends on timing of writing to transmit buffer.

3. Software Countermeasures

(1) In order to eliminate the influence of the delay of the cycle when the first data transfer is available, please set Transmit enable bit (TE) and/or Receive bit (RE) 256 cycles (of BRG count source) after setting UiBRG. Since underflows except the first time are generated during the expected cycle, the delay of the first underflow of BRG does not affect the cycle when data transfer is available.

(2) If case (1) above is impossible, please set UiBRG to any value except '00h'. The delay of the first underflow of BRG will not occur.

If case (1) or (2) above is implemented, M30245MC/8-XXXGP and M30245FCGP behaves in the same way.

4. Hardware Countermeasures

M30245MC/8-XXXGP will be revised. The new revision of the chip will be available for ROM ordering in Nov. 2003. If case (1) or (2) above is implemented, two revisions of the chip behaves in the same way.