To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-16C-A162A/E	Rev.	1.00
Title	M16C/80 Series, M32C/80 Series Usage Precaution for Clock synchronous serial I/O mode in Serial interfaces (Serial I/O)		Information Category	Technical Notification		
Applicable Product	M16C/80, M32C/80, M32C/81, M32C/82, M32C/83, M32C/84, M32C/85, M32C/86, M32C/87, M32C/88 Groups	Lot No.	Reference Document			

1. Precaution

UARTi in serial interfaces (Serial I/O) may start unintended data reception when all of the following three conditions are met. (i = 0 to 4, except i = 0 to 6 in M32C/87)

(1) Bits SMD2 to SMD0 in the UiMR register are set to 001b (Clock synchronous serial I/O mode)

(2) When either of these conditions is met

a) The CKDIR bit in the UiMR register is set to 0 (Internal clock)

b) When the CKDIR bit is set to 1 (External clock), the CRD bit in the UiC0 register is set to 0 and the CRS bit in the UiC0 register is set to 1 (Select $\overline{\text{RTS}}$ function)(1)

(3) The UiRRM bit in registers UiC1, UCON, or U56CON is set to 1 (Continuous receive mode enabled)

UCON register: UARTi in M16C/80 (i = 0 and 1)

U56CON register: UARTi in M32C/87 (i = 5 and 6)

UiC1 register: all the UARTi other than the above

NOTE:

1. This problem does not occur unless the $\overline{\text{RTS}}$ function is used, regardless of external clock selection.

2. Countermeasures

When using under the conditions of (1) and (2), set the UiRRM bit in the corresponding register to 0 (continuous receive mode disabled). Also, write dummy data to the UiTB register every time a receive operation has completed, using an interrupt generated at the completion of the receive operation.