To our customers,

Old Company Name in Catalogs and Other Documents

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GRADE A

MESC TECHNICAL NEWS No.M16C-42-0001

M16C/80 Group Cautions for Interrupt Control Register

1. Affected devices

- M16C/80 Group

2. Cautions

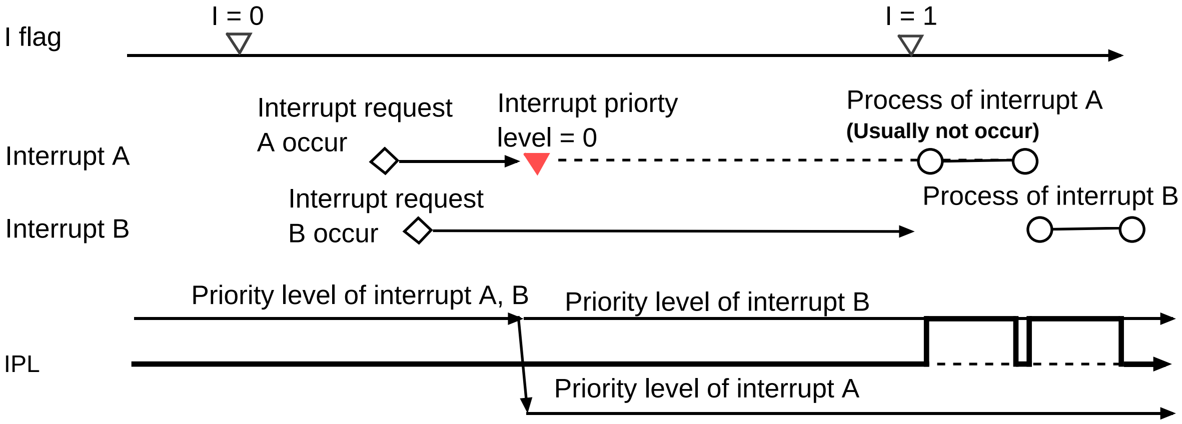
There is the possibility of an interrupt occurring even if the interrupt is disabled and the interrupt request bit is cleared, under the following conditions:

2.1 When interrupt flag I = 0 (Interrupt disabled) and ‘Interrupt A’ is disabled by changing the interrupt priority level to ‘0’ or lower than the ‘processor interrupt priority level (IPL)‘, the MCU may still execute ‘Interrupt A’ after the ‘I’ flag is set to 1 (Interrupt enabled), if the following conditions are met:

(1) In the case where ‘Interrupt A’ which is going to be modified the priority level and interrupt ‘B’ have the same interrupt priority level which is higher than the current IPL.

(2) The order of the interrupt requests are ‘Interrupt A’->‘Interrupt B’.
Or ‘Interrupt A’ and ‘Interrupt B’ occur at same time but A has a higher Peripheral I/O interrupt priority (please see the ‘Interrupt‘ chapter of the manual for more information).

(3) The priority level is changed to ‘0’ or lower than IPL after (2).

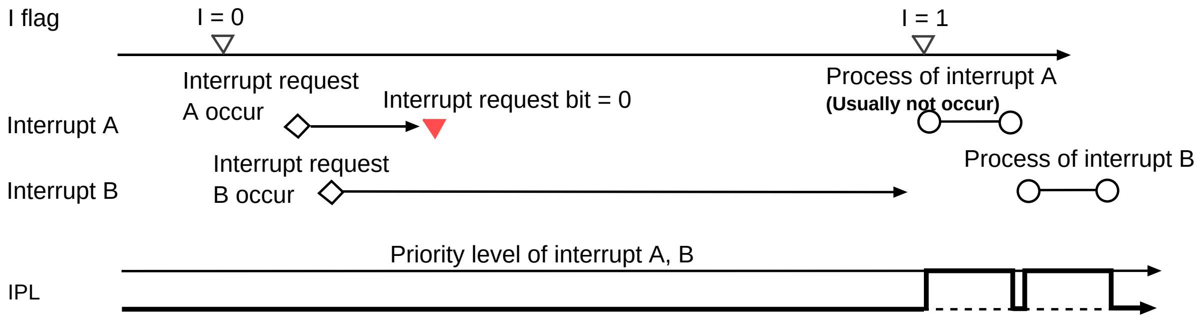

I flag
I = 0
I = 1
Interrupt A
Interrupt request A occur
Interrupt priorty level = 0
Process of interrupt A
(Usually not occur)
Interrupt B
Interrupt request B occur
Process of interrupt B
IPL
Priority level of interrupt A, B
Priority level of interrupt B
Priority level of interrupt A

2.2 When I flag = 0 (Interrupt disabled) and the request bit of ‘Interrupt A’ is cleared to ‘0’, the MCU may still execute ‘Interrupt A’ after the ‘I’ flag is set to 1 (Interrupt enabled), if the following conditions are met:

(1) In the case where ‘Interrupt A’ which is going to be cleared the request bit and interrupt ‘B’ have the same interrupt priority level which is higher than the current IPL.

(2) The order of the interrupt requests are ‘Interrupt A’->‘Interrupt B’.
Or ‘Interrupt A’ and ‘Interrupt B’ occur at same time but A has a higher Peripheral I/O interrupt priority (please see the ‘Interrupt‘ chapter of the manual for more information).

(3) The Interrupt Request bit of ‘Interrupt A’ is cleared after (2).



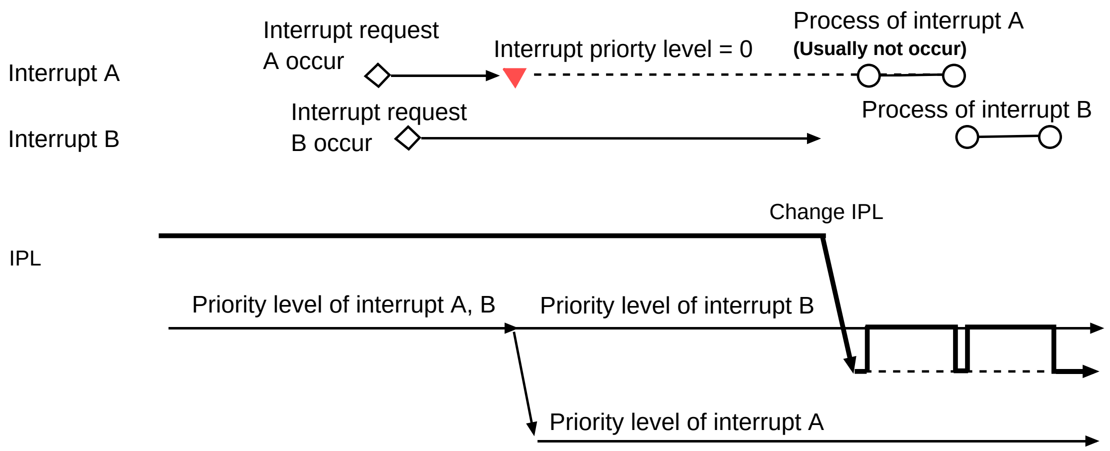
2.3 When the interrupt priority level of ‘Interrupt A’ and ‘Interrupt B’ is lower than IPL and the priority level of ‘interrupt A’ is changed to ‘0’ or lower than the current priority level, the MCU may still execute ‘interrupt A’, if the following conditions are met:

(1) In the case where ‘Interrupt A’ which is going to be modified the priority level and interrupt ‘B’ have the same interrupt priority level which is lower than the current IPL, but not ‘0’.

(2) The order of the interrupt requests are ‘Interrupt A’->‘Interrupt B’.
Or ‘Interrupt A’ and ‘Interrupt B’ occur at same time but A has a higher Peripheral I/O interrupt priority (please see the ‘Interrupt‘ chapter of the manual for more information).

(3) The priority level is changed to ‘0’ or lower than IPL after (2).

(4) The IPL is changed to a lower level than the initial ‘Interrupt A’ priority level but higher than the current level after (3).


Interrupt A
Interrupt B
Interrupt request A occur
Interrupt priorty level = 0
Process of interrupt A
(Usually not occur)
Interrupt request B occur
Process of interrupt B
Change IPL
IPL
Priority level of interrupt A, B
Priority level of interrupt B
Priority level of interrupt A

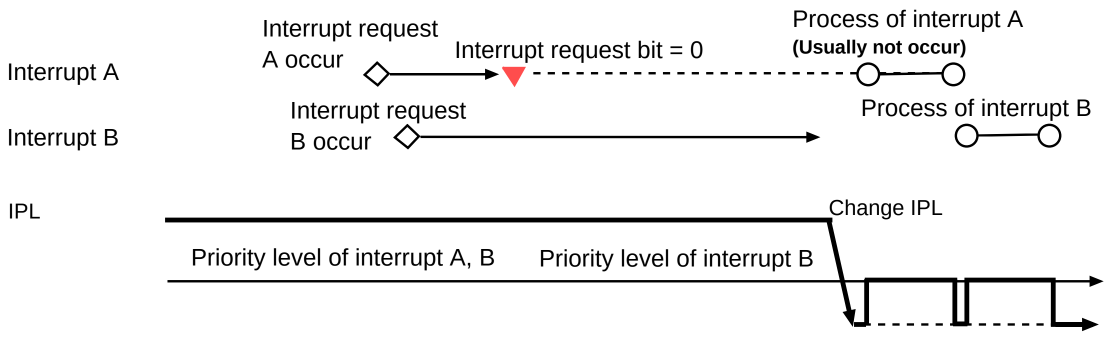
2.4 When the interrupt priority level is lower than IPL and the interrupt request bit is cleared, the MCU may still execute 'interrupt A', if the following conditions are met:

(1) In the case where 'Interrupt A' which is going to be cleared the request bit and interrupt 'B' have the same interrupt priority level which is lower than the current IPL, but not '0'.

(2) The order of the interrupt requests are 'Interrupt A'->'Interrupt B'.
Or 'Interrupt A' and 'Interrupt B' occur at same time but A has a higher Peripheral I/O interrupt priority (please see the 'Interrupt' chapter of the manual for more information).

(3) The Interrupt Request bit of 'Interrupt A' is cleared after (2).

(4) The IPL is changed to a lower level than the initial 'Interrupt A' and 'B' priority level.


Interrupt A
Interrupt B
Interrupt request A occur
Interrupt request bit = 0
Process of interrupt A
(Usually not occur)
Interrupt request B occur
Process of interrupt B
IPL
Change IPL
Priority level of interrupt A, B
Priority level of interrupt B

3. Countermeasure

3.1 If you have the following conditions, you do not need to perform countermeasures.

(1) With the interrupt disabled, you do not rewrite interrupt priority level to ‘0’ (or lower than IPL) or do not clear the interrupt request bit to ‘0’.

(2) You rewrite the interrupt priority level to ‘0’ (or lower than IPL) or clear the interrupt request bit to ‘0’ with the interrupt disabled, but there is no other interrupt with the same priority level.

(3) When rewriting the interrupt priority level to ‘0’ (or lower than IPL) or clearing the interrupt request bit to ‘0’ with the interrupt disabled, there is no corresponding interrupt request (e.g.: Timer is stopped).

3.2 If you have conditions not listed above, please use the following countermeasures:

(1) If you change the interrupt priority level to ‘0’ (or lower than IPL) or clear the interrupt request bit to ‘0’ when flag I = ‘0’ (interrupt disabled), first change the priority level to higher than the current level so it is not at the same level as others interrupts, and then later change to ‘0’ (or lower level).

However, when you change an interrupt priority level to higher than the current level, you have to use ‘AND’ and ‘OR’ instruction to avoid clearing the request flag.

For example, if you use level ‘6’ for temporary priority level and disable the interrupt, there will be no problem when you change priority level from ‘6’ down to ‘0’.

Ex. In case of Timer A0 priority level change to ‘0’

```
AND.B    #11111110b,TA0IC
OR.B     #00000110b,TA0IC     ; Set the Timer A0 priority levels to 6
MOV.B    #00000000b,TA0IC     ; Set the Timer A0 priority levels to 0
```

(2) When you change interrupt priority level to ‘0’, lower than current level or clear the interrupt request bit, set a priority level that it is not the same as priority levels of the other interrupts.

(3) Read the priority level of each interrupt control register during the interrupt service routine.
If the level is ‘0’, please ignore and return.