Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-16C-A157A/E	Rev.	1.00
Title	M16C/70 Series, M16C80 Series, M Series, M32C/90 Series: Usage Precaution for String Instructi Sum Operation Instruction		Information Category	Technical Notification		
Applicable Product	M16C/70, M16C/80,M32C/80, M32C/81, M32C/82, M32C/83, M32C/84, M32C/85, M32C/86, M32C/87, M32C/88, M32C/95 Groups	Lot No.	Reference Document			

1. Precaution

The string instructions and the product sum operation instruction listed in **1.1 Subject Instructions** will be aborted under the conditions listed in **1.2 Problem Conditions**.

1.1 Subject Instructions

String instructions: SCMPU, SIN, SMOVB, SMOVF, SMOVU, SOUT, SSTR Product sum operation instruction: RMPA

1.2 Problem Conditions

When DMAC is not used:

- (a) The interrupt A is requested when bits ILVL2 to ILVL0 in the interrupt control registers are set to other than 000b (level 0, interrupt disabled). However, the interrupt request is not acknowledged because the I flag is set to 0 (interrupt disabled) or the requested interrupt has smaller priority level than IPL (IPL interrupt priority level < 001b) while the interrupt is requested.
 - (b) After (a), set the IR bit in the interrupt control register for the interrupt A to 0 (no interrupt request) by program or set the interrupt priority level smaller than the last set level.
 - (c) After (b), execute the subject instruction, SCMPU, SIN, SMOVB, SMOVF, SMOVU, SOUT, SSTR, or RMPA, immediately after setting the I flag to 1 or IPL to smaller priority than the interrupt priority level, which is set when an interrupt request is generated, to enable the requested interrupt.

When DMAC is used,

- 2) (a) The interrupt A is requested when bits ILVL2 to ILVL0 are set to other than 000b. However, the interrupt request is not acknowledged because the I flag is set to 0 or the requested interrupt has smaller priority level than IPL (IPL interrupt priority level < 001b) while the interrupt is requested.</p>
 - (b) After (a), set the IR bit for the interrupt A to 0 by program or set the interrupt priority level smaller than the last set level.
 - (c) After (b), execute the subject instruction within next three instructions after setting the I flag to 1 or IPL to smaller priority than the interrupt priority level, which is set when an interrupt request is generated, to enable the requested interrupt.
- 3) (a) Interrupts are generated immediately before or in the middle of executing the subject instruction. The interrupt A request is generated when bits ILVL2 to ILVL0 are set to other than 000b (level 0, interrupt disabled) in the interrupt routine. However, the interrupt request is not acknowledged because I flag is set to 0 or because IPL is equal to or greater than the interrupt priority level even if I flag is set to 1 (multipul interrupts enabled).
 - (b) After (a), set the IR bit for the interrupt A to 0 by program or set the interrupt priority level smaller than the last set level.
 - (c) After (b), execute the subject instructions after the interrupts are completed with the REIT instruction or FREIT instruction.

If DMA transfer occurs in conditions 2)-(c) or 3)-(c), the subject instruction is aborted. The patterns for the above conditions 1) through 3) are illustrated in **Figure 1**.

2. Operation Check

Use the flow chart in **Figure 2** to determine whether the countermeasure programs are needed. When the countermeasure is needed, refer to **3. Countermeasure Program**.

3. Countermeasure Program

To execute the subject instruction, interrupts need to be disabled. If interrupts cannot be disabled, use the countermeasure program in **Figure 3**.

:			 Interrupt disabled 	
Interrup	t A request is	generated	– IR bit is set to 1 (interrupt requested)	≻ (a)
: mov.b :	#3, interrupt	control register for the interrupt A	 Set the IR bit to 0 (interrupt not requested) 	(b)
mov.w fset Subject	#0, R0 I •	<	Interrupt enabledSubject instructions aborted	≻ (c)
ondition I				
fclr	I	•	- Interrupt disabled	≻ (a)
Interrupt	A request is	enerated	 IR bit is set to 1 (interrupt requested) 	~ (a)
: mov.b :	#3, interrupt	control register for the interrupt A \blacktriangleleft	 Set the IR bit to 0 (interrupt not requested) 	(b)
mov.w fset nop	#0, R0 I	← DMA transfer is generated at this	 Interrupt enabled 	≻ (c)
	nstructions	timing 🗸	 Subject instructions aborted 	
fset : mov.w	I #0 , R0		mmediately before or in the middle of sub ne interrupt routine, I flag is set to 0 (inter	
mov.w mov.w :	#addr, A1 #cycl, R3	Interrupt (I = 0)) (a)	
Subject	instructions -	Interrupt A request is ge	nerated	
Subj abor	ect instructio			(b)
ondition I	II			
e 1. Pro	blem Cond	itions		





Loop:				
•	nstruction			
cmp.w	#0, R3			
jnz	Loop			
SMOVU Inst		•SCMPU Instruction		
	ize specifier is ".B,"	When the size specifier is ".B,"		
Loop:		Loop:		
smovu.		scmpu.b		
sub.l	#1, A0	pushc	FLG	
sub.l	#1, A1	jnz	Next	
cmp.b	#0, [A0]	sub.l	#1, A0	
jnz	Loop	sub.l	#1, A1	
		cmp.b	#0, [A0]	
When the s	ize specifier is ".W,"	jz	Next	
Loop:		рорс	FLG	
smovu.w		jmp	Loop	
sub.l	#1, A0	Next:	-	
sub.l	#1, A1	рорс	FLG	
cmp.b	#0, [A0]			
jz Next		When the size s	pecifier is ".W,"	
sub.l	#1, A0	Loop:		
sub.l	#1, A1	scmpu.w		
cmp.b	#0, [A0]	pushc	FLG	
jnz	Loop	jnz	Next	
Nex:	•	sub.l	#1, A0	
		sub.l	#1, A1	
RMPA Instruction		cmp.b	#0, [A0]	
Loop:		jz	Next	
rmpa.b (rmpa.w)		, sub.l	#1, A0	
pushc	FLG	sub.l	#1, A1	
jz	Next	cmp.b	#0, [A0]	
popc	FLG	jz	Next	
jmp	Loop	popc	FLG	
Next:	- F	jmp	Loop	
рорс	FLG	Next:	p	
Popo	0	рорс	FLG	

Figure 3. Countermeasuer Programs

