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On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A178A/E	Rev.	1.00
Title	M16C/65, M16C/64A Groups Serial Interface CLK Pin Note on Selecting N-channel Open Drain Output		Information Category	Technical Notification		
Applicable Products	M16C/65, M16C/64A Groups	Lot No.	Reference Documents			
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This document describes a note on using the N-channel open drain output as an output mode of the CLKi pin for serial interface UARTi (i = 0 to 2, 5 to 7).
In this document, port Px_x represents the port which shares a pin with CLKi. (Refer to 3. Target Pins)

1. Note

The Px_x/CLKi pin is high-impedance when using this bit as an input port. However, the Px_x/CLKi pin outputs a low-level signal regardless of a value in the direction register of the port Px_x when the following three conditions are met:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The NODC bit in the UiSMR3 register is 1 (CLKi is N-channel open drain output).
- The Px_x bit in the Px register is 0 (output low level).

2. Countermeasures

Set the bits using the following procedures:
When changing the pin function from port Px_x to CLKi.
(1) Set bits SMD2 to SMD0 to a value other than 000b to select serial interface mode.
(2) Set the NODC bit to 1.

When changing the pin function from CLKi to port Px_x.
(1) Set the NODC bit to 0.
(2) Set bits SMD2 to SMD0 to 000b to disable the serial interface.

3. Target Pins

Target pins are the CLKi pins for serial interface UARTi:
P6_1/CLK0, P6_5/CLK1, P7_2/CLK2, P7_7/CLK5, P1_1/CLK6, P4_5/CLK7

(CLK3 and CLK4 pins of serial interface SI/O3 and SI/O4 are not included.)