To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

GRADE A

MESC TECHNICAL NEWS No.M16C-18-9902

M16C/62 Group
Precautions for UART2 Special Mode register

1. Related devices

M16C/62 group

2. Precautions

The UART2 special mode register (address 0377_{16}:U2SMR) is used to control various functions of UART2.
In previous tentative specifications, it is mentioned "Nothing is assigned in the bit 7 of this register."
However, bit 7 is reserved for expansion of IIC circuit function.
Therefore when writing to U2SMR, clear bit 7 to 0.

UART2 special mode register (address 0377_{16}) is shown by figure 1.

UART2 Special Mode register

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol U2SMR — Address 0377_{16} — When reset 00_{16}

Bit symbol	Bit name	Function (During clock synchronous serial I/O mode)	Function (During UART mode)	R	W
IICM	I^2C mode selection bit	0 : Normal mode 1 : I^2C mode	Must always be “0”	○	○
ABC	Arbitration lost detecting flag control bit	0 : Update per bit 1 : Update per byte	Must always be “0”	○	○
BBS	Bus busy flag	0 : STOP condition detected 1 : START condition detected	Must always be “0”	○	○ (Note)
LSYN	SCLL sync output enable bit	0 : Disabled 1 : Enabled	Must always be “0”	○	○
ABSCS	Bus collision detect sampling clock select bit	Must always be “0”	0 : Rising edge of transfer clock 1 : Underflow signal of timer A0	○	○
ACSE	Auto clear function select bit of transmit enable bit	Must always be “0”	0 : No auto clear function 1 : Auto clear at occurrence of bus collision	○	○
SSS	Transmit start condition select bit	Must always be “0”	0 : Ordinary 1 : Falling edge of RxD2	○	○
Reserved bit		Must always be set to “0”.		–	○

Note: Nothing but "0" may be written.

Figure 1. UART2 Special Mode register