

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-SY*-A033A/E	Rev.	1.00
Title	Limitations on programming the Option-Setting Memory for flash access applications		Information Category	Technical Notification	
Applicable Product	Renesas Synergy™ S5D5 MCU Group Renesas Synergy™ S5D9 MCU Group	Lot No.	Reference Document	S5D5 Microcontroller Group User's Manual: Rev.1.10 S5D9 Microcontroller Group User's Manual: Rev.1.10	
		All lots			

This TU describes limitations and constraints for the Renesas Synergy S5 series devices that must be followed. Refer to the Microcontroller Group User's Manuals (UMs) in the Reference Document section. The Option-Setting Memory is in Chapter 7 of the related MCU UM, and it describes the state of the MCU after reset, and available methods for programming the related registers (OFS0, OFS1, AWS, and OCD/OSIS). Additionally, the details for programming the Option-Setting Memory is described in section **7.3.2 Setting Data for Programming the Option-Setting Memory** of the MCU UM. Additional text (in red) added to section 7.3.2 describes the details of the limitations and restrictions that must be followed.

[Information from the S5 series MCU UM]

7.3.2 Setting Data for Programming the Option-Setting Memory

Allocating data as described in [section 7.3.1, Allocation of Data in the Option-Setting Memory](#) does not alone result in the data being written to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

To write data to the program flash area, use the programming command. To write data to the option-setting memory in the configuration setting area, use the configuration setting command. In addition, use startup area select function to safely update the boot program that includes the option-setting memory.

For details on the programming command, the configuration setting command, and the startup area select function, see [section 55, Flash Memory](#). See Note ^{*1}.

WARNING: While programming the configuration setting area, the code must not execute at or access (from CPU, DMAC/DTC, EDMAC, LCDC/DRW/JPEG) addresses that satisfy the ranges described by the expression defined in **Expression 1** on the following page. Also, the functions provided by the Renesas Synergy™ Software Package (SSP) to program AWS will not execute in addresses that satisfy the ranges described by the expression defined in **Expression 1**.

Note: Interrupts are allowed, however, the ISR must be prevented from executing or accessing any addresses that satisfy the ranges described by the expression defined in **Expression 1**. It is highly recommended that you disable all interrupts, and the DMAC/DTC, EDMAC, LCDC/DRW/JPEG while programming the configuration setting area because the interrupts and these modules might access prohibited area in **Expression 1**. See Note ^{*2}.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, so refer to the tool manual for details. There are two setting procedures:

- *Read the data, allocated as described in [section 7.3.1, Allocation of Data in the Option-Setting Memory](#), from an object file or Motorola S-format file generated by the compiler, then write the data to the MCU

- *Use the GUI interface of the tool to program the same data, allocated as described in [section 7.3.1, Allocation of Data in the Option-Setting Memory](#).

WARNING: While programming the OSIS or AWS register, the code must not access (from CPU, DMAC/DTC, EDMAC, LCDC/DRW/JPEG) or execute at addresses that satisfy the ranges described by the expression defined in **Expression 1**. See Note ^{*2}.

Expression 1:

If (((address & 0x0101F800) == 0x01010000) || ((address & 0x0101FC00) == 0x01012000))

To help with decoding the impacted memory space, you can use the following address map for the S5 series to determine if, in fact, the flash access code in the application is within the restricted areas.

- **Restricted areas:** SDRAM, CS, SPI, and SRAMHS.
- **None restricted areas:** System for the Cortex-M4, flash I/O registers, option setting memory, data flash, peripheral I/O registers, Standby SRAM, SRAM0, memory mapping area, and program flash.

For example, the ranges of addresses 0x1FFF0000 to 0x1FFF07FF or 0x1FFF2000 to 0x1FFF23FF are associated with the SRAMHS area that is tagged as restricted.

Synergy S5D5 MCU address map

FFFF FFFFh	System for Cortex®-M4
E000 0000h	Reserved area
9800 0000h	External address space (SDRAM area)
9000 0000h	Reserved area
8720 0000h	External address space (CS area)
8000 0000h	Reserved area
6800 0000h	External address space (SPI area)
6000 0000h	Reserved area
4080 0000h	Flash I/O registers
407F C000h	Reserved area
407F B1A0h	On-chip flash (option-setting memory)
407F B19Ch	Reserved area
407F 0000h	Flash I/O registers
407E 0000h	Reserved area
4010 8000h	On-chip flash (data flash)
4010 0000h	Peripheral I/O registers
4000 0000h	Reserved area
2010 0000h	Standby SRAM
200F E000h	Reserved area
2004 0000h	On-chip SRAM
1FFE 0000h	Reserved area
0280 0000h	Memory mapping area
0200 0000h	Reserved area
0100 A168h	On-chip flash (option-setting memory)
0100 A150h	Reserved area
0100 8000h	On-chip flash (option-setting memory)
0100 7000h	Reserved area
0010 0000h	On-chip flash (program flash) (read only)
0000 0000h	

Synergy S5D9 MCU address map

FFFF FFFFh	System for Cortex®-M4
E000 0000h	Reserved area
9800 0000h	External address space (SDRAM area)
9000 0000h	Reserved area
8800 0000h	External address space (CS area)
8000 0000h	Reserved area
6800 0000h	External address space (SPI area)
6000 0000h	Reserved area
4080 0000h	Flash I/O registers
407F C000h	Reserved area
407F B1A0h	On-chip flash (option-setting memory)
407F B19Ch	Reserved area
407F 0000h	Flash I/O registers
407E 0000h	Reserved area
4011 0000h	On-chip flash (data flash)
4010 0000h	Peripheral I/O registers
4000 0000h	Reserved area
2010 0000h	Standby SRAM
200F E000h	Reserved area
2004 0000h	SRAM0
2000 0000h	SRAMHS area
1FFE 0000h	Reserved area
0280 0000h	Memory mapping area
0200 0000h	Reserved area
0100 A168h	On-chip flash (option-setting memory)
0100 A150h	Reserved area
0100 8000h	On-chip flash (option-setting memory)
0100 7000h	Reserved area
0020 0000h	On-chip flash (program flash) (read only)
0000 0000h	

The Renesas Synergy Software Package (SSP 1.5.0-MP and later) includes these restrictions within the appropriate APIs. It also provides a runtime check-and-fail if the code that programs the configuration setting area through appropriate APIs violates the described restrictions.

Notes:

*1) In the S5D5 MCU, section 53.

*2) There are no LCDC/DRW/JPEG in the S5D5 MCU

Please contact your Renesas sales person or Customer Support for further details and information on how to download and install the software workaround.

Technical Support:

renesassynergy.com/support