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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	9th, December, 1997	No.	TN-SH7-083 A/E
THEME	Limitations of H8S/2148 Series E6000 Emulator		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents ☒ Limitation on Use		
PRODUCT NAME	HS2148EPI60H	Lot No. etc.	All
REFERENCE DOCUMENT	H8S/2148 Series E6000 Emulator User's Manual (HS2148EPI60HE)	Effective Date	Permanent
		From	November 10th, 1997

The H8S/2148 evaluation chip used in the H8S/2148 series E6000 emulator has the restrictions described on the following pages. Read and understand the restrictions that apply to the device used.

Target Device: H8S/2148 Series

No.	Item	Product Chip and Hardware Manual Descriptions	Emulator	Notes and Solutions for Development
1	Data output from ports 2 and A by IOSE bit in advanced modes	In advanced mode 2, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) and port A (PA0 to PA7) can be used for data output. In advanced mode 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for data output.	Not supported. In advanced mode 2, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) and port A (PA0 to PA7) can be used for address output. In advanced mode 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for address output.	If data output ports are necessary, temporarily use other ports.
2	Interrupt mask of address break	Interrupt is not masked depending on I bit of CCR.	Interrupt is masked depending on I bit of CCR.	Be sure to set an address break in an area not containing an interrupt mask set by the program.
3	HIE bit restriction, and pull-up and key-input interrupt functions of port 6	HIE bit is used for selecting registers multiplexed to the same address.	HIE bit is used not only for selecting registers multiplexed to the same address but for switching from single-chip mode to slave mode.	Note that when HIE bit is set to 1 in single-chip mode, the emulator transfers to slave mode. This is the same when the pull-up or key-input interrupt function of port 6 is used.
4	HI12E bit of SYSCR2 register	HI12E bit of the SYSCR2 register controls the internal host interface. When clearing the module stop bit of the host interface in single-chip mode and setting the HI12E bit to 1, slave mode is entered.	The SYSCR2 register cannot be accessed. When the host interface is used, the emulator can operate in slave mode by clearing the module stop bit of the host interface and setting HIE bit of the SYSCR register to 1.	When the host interface is used, set HI12E bit of the SYSCR2 register to 1 (dummy write). Do not read or judge this register, since it cannot be accessed by the evaluation chip.
5	HSYNCO output selection (P44) of timer connection	Regardless of OS3 to OS0 bits of TCSR in TMR1, and OS3 to OS0 bits of TCSR in TMRX, the HSYNCO pin can be used for output.	OS3 to OS0 bits of TCSR in TMR1, and OS3 to OS0 bits of TCSR in TMRX must be set to 0, to use the HSYNCO pin for output.	Set OS3 to OS0 bits of TCSR in TMR1, and OS3 to OS0 bits of TCSR in TMRX to 0, to use the HSYNCO pin for output.
6	Assertion/ negation conflict of cramped signal of timer connection	—	When satisfaction of an output condition of a cramped signal conflicts with the second-or-more occurrence of a compare match signal, the cramped signal may become an abnormal waveform.	Adjust the cramped signal width or change the compare match timing to set conditions that do not conflict.
7	Flag set/read conflict of timer connection register	—	When the flag set and read of a timer connection register conflicts, the register clear condition which is data 1 read from the flag may not be recognized.	To be sure to clear the flag, read data 1 twice or read data 1 again before clearing if the register is not cleared at the first time.

Target Device: H8S/2144 Series

No.	Item	Product Chip and Hardware Manual Descriptions	Emulator	Notes and Solutions for Development
1	Data output from ports 2 and A by IOSE bit in advanced modes	In advanced mode 2, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) and port A (PA0 to PA7) can be used for data output. In advanced mode 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for data output.	Not supported. In advanced mode 2, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) and port A (PA0 to PA7) can be used for address output. In advanced mode 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for address output.	If data output ports are necessary, temporarily use other ports.
2	Interrupt mask of address break	Interrupt is not masked depending on I bit of CCR.	Interrupt is masked depending on I bit of CCR.	Be sure to set an address break in an area not containing an interrupt mask set by the program.
3	Access to TMRY bit of TCONRS register	TMRX/Y bit of the TCONRS register can never be 1; the TCONRS register can be accessed by setting MSTP8 = 0 and HIE = 0.	In addition to setting MSTP8 = 0 and HIE = 0, TMRX/Y bit of the TCONRS register must be set to 1.	Because the timer connection functions must be enabled, set the target device of the emulator to H8S/2148 series. Then set TMRX/Y bit of the TCONRS register to 1 (dummy write). Do not read or judge this register in the program, since it cannot be accessed by the product chip.

Target Device: H8S/2138 Series

No.	Item	Product Chip and Hardware Manual Descriptions	Emulator	Notes and Solutions for Development
1	Data output from port 2 by IOSE bit in advanced modes	In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for data output.	Not supported. In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for address output.	If data output ports are necessary, temporarily use other ports.
2	Interrupt mask of address break	Interrupt is not masked depending on I bit of CCR.	Interrupt is masked depending on I bit of CCR.	Be sure to set an address break in an area not containing an interrupt mask set by the program.
3	HIE bit restriction, and pull-up and key-input interrupt functions of port 6	HIE bit is used for selecting registers multiplexed to the same address.	HIE bit is used not only for selecting registers multiplexed to the same address but for switching from single-chip mode to slave mode.	Note that when HIE bit is set to 1 in single-chip mode, the emulator transfers to slave mode. This is the same when the pull-up or key-input interrupt function of port 6 is used.
4	HI12E bit of SYSCR2 register	HI12E bit of the SYSCR2 register controls the internal host interface. When clearing the module stop bit of the host interface in single-chip mode and setting the HI12E bit to 1, slave mode is entered.	The SYSCR2 register cannot be accessed. When the host interface is used, the emulator can operate in slave mode by clearing the module stop bit of the host interface and setting HIE bit of the SYSCR register to 1.	When the host interface is used, set HI12E bit of the SYSCR2 register to 1 (dummy write). Do not read or judge this register, since it cannot be accessed by the evaluation chip.
5	HSYNCO output selection (P44) of timer connection	Regardless of OS3 to OS0 bits of TCSR in TMR1, and OS3 to OS0 bits of TCSR in TMRX, the HSYNCO pin can be used for output.	OS3 to OS0 bits of TCSR in TMR1, and OS3 to OS0 bits of TCSR in TMRX must be set to 0, to use the HSYNCO pin for output.	Set OS3 to OS0 bits of TCSR in TMR1, and OS3 to OS0 bits of TCSR in TMRX to 0, to use the HSYNCO pin for output.
6	CBLANK signal output condition of timer connection	The CBLANK signal is made from the OR of four inputs: HFBACKI signal, VFBACKI signal, IVO signal, and the output of RS-F/F which is set at the falling-edge of the VFBACKI signal and reset at the rising-edge of the IVO signal.	The CBLANK signal is made from the OR of four inputs: HFBACKI signal, VFBACKI signal, IVO signal, and the output of RS-F/F which is set at the falling-edge of the VFBACKI signal and reset at the rising-edge of the IVO signal.	In the emulator mounted with the current evaluation chip, the CBLANK signal output of timer connection is not supported.
7	Assertion/ negation conflict of cramped signal of timer connection	—	When satisfaction of an output condition of a cramped signal conflicts with the second-or-more occurrence of a compare match signal, the cramped signal may become an abnormal waveform.	Adjust the cramped signal width or change the compare match timing to set conditions that do not conflict.
8	Flag set/read conflict of timer connection register	—	When the flag set and read of a timer connection register conflicts, the register clear condition which is data 1 read from the flag may not be recognized.	To be sure to clear the flag, read data 1 twice or read data 1 again before clearing if the register is not cleared at the first time.

Target Device: H8S/2134 Series

No.	Item	Product Chip and Hardware Manual Descriptions	Emulator	Notes and Solutions for Development
1	Data output from port 2 by IOSE bit in advanced modes	In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for data output.	Not supported. In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for address output.	If data output ports are necessary, temporarily use other ports.
2	Interrupt mask of address break	Interrupt is not masked depending on I bit of CCR.	Interrupt is masked depending on I bit of CCR.	Be sure to set an address break in an area not containing an interrupt mask set by the program.
3	Access to TMRY bit of TCONRS register	TMRX/Y bit of the TCONRS register can never be 1; the TCONRS register can be accessed by setting MSTP8 = 0 and HIE = 0.	In addition to setting MSTP8 = 0 and HIE = 0, TMRX/Y bit of the TCONRS register must be set to 1.	Because the timer connection functions must be enabled, set the target device of the emulator to H8S/2138 series. Then set TMRX/Y bit of the TCONRS register to 1 (dummy write). Do not read or judge this register in the program, since it cannot be accessed by the product chip.

Target Device: H8S/2128 Series

No.	Item	Product Chip and Hardware Manual Descriptions	Emulator	Notes and Solutions for Development
1	Data output from port 2 by IOSE bit in advanced modes	In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for data output.	Not supported. In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for address output.	If data output ports are necessary, temporarily use other ports.
2	Interrupt mask of address break	Interrupt is not masked depending on I bit of CCR.	Interrupt is masked depending on I bit of CCR.	Be sure to set an address break in an area not containing an interrupt mask set by the program.
3	HSYNCO output selection (P67) of timer connection	Regardless of OS3 to OS0 bits of TCSR in TMRX, the HSYNCO pin can be used for output.	OS3 to OS0 bits of TCSR in TMRX must be set to 0, to use the HSYNCO pin for output.	Set OS3 to OS0 bits of TCSR in TMRX to 0, to use the HSYNCO pin for output.
4	Assertion/ negation conflict of cramped signal of timer connection	—	When satisfaction of an output condition of a cramped signal conflicts with the second-or-more occurrence of a compare match signal, the cramped signal may become an abnormal waveform.	Adjust the cramped signal width or change the compare match timing to set conditions that do not conflict.
5	Flag set/read conflict of timer connection register	—	When the flag set and read of a timer connection register conflicts, the register clear condition which is data 1 read from the flag may not be recognized.	To be sure to clear the flag, read data 1 twice or read data 1 again before clearing if the register is not cleared at the first time.

Target Device: H8S/2124 Series

No.	Item	Product Chip and Hardware Manual Descriptions	Emulator	Notes and Solutions for Development
1	Data output from port 2 by IOSE bit in advanced modes	In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for data output.	Not supported. In advanced modes 2 and 3, if DDR = 1 and IOSE bit = 1 are set, port 2 (P24 to P27) can be used for address output.	If data output ports are necessary, temporarily use other ports.
2	Interrupt mask of address break	Interrupt is not masked depending on I bit of CCR.	Interrupt is masked depending on I bit of CCR.	Be sure to set an address break in an area not containing an interrupt mask set by the program.
3	Access to TMRY bit of TCONRS register	TMRX/Y bit of the TCONRS register can never be 1; the TCONRS register can be accessed by setting MSTP8 = 0 and HIE = 0.	In addition to setting MSTP8 = 0 and HIE = 0, TMRX/Y bit of the TCONRS register must be set to 1.	Because the timer connection functions must be enabled, set the target device of the emulator to H8S/2128 series. Then set TMRX/Y bit of the TCONRS register to 1 (dummy write). Do not read or judge this register in the program, since it cannot be accessed by the product chip.