To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	Development environment		No	TN-EML-093A/E	Rev.	1
THEME	Limitation on Using the H8S/2678, 2678R, 2668, 2368, and 2378 E6000 Emulator	Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use		4. Change of Mask 5. Change of Production Line	
PRODUCT NAME	HS2678REPI61H	Lot No. See below.	Reference Documents	H8S Series E6000 Emulator ADE-702-194B	Effective Date Permanent	

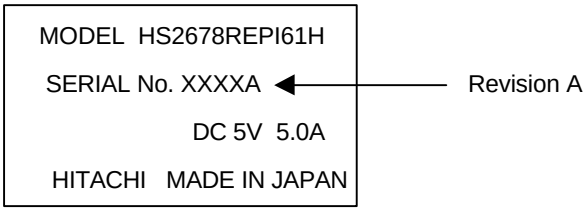
In the H8S/2678, 2678R, 2668, 2368, and 2378 series E6000 emulator HS2678REPI61H, there are following limitations. These limitations apply to emulation of the H8S/2368 and H8S/2378 series microcomputer, and not to emulation of the H8S/2678, H8S/2678R, and H8S/2668 series microcomputer.

If you need to modify the emulator, contact Hitachi's sales agency.

1. Target Product Revisions (For details, refer to the following pages.)

No.	Limitation	Emulator Revision	Microcomputer
(1)	IIC bus interface 1	A	H8S/2378, 2368 series
(2)	Port 9	A	H8S/2378 series
(3)	IIC bus interface 2	A and B	H8S/2378, 2368 series

The product revision is written on the label on the back of the emulator station.



2. Limitations

2-1 IIC Bus Interface 1

(1) Limitation on issuing the halt condition

When there is a slave device that inserts a wait by driving SCL at the low level, issue the halt condition after the slave device has released SCL. The halt condition is not correctly issued during the low period of SCL.

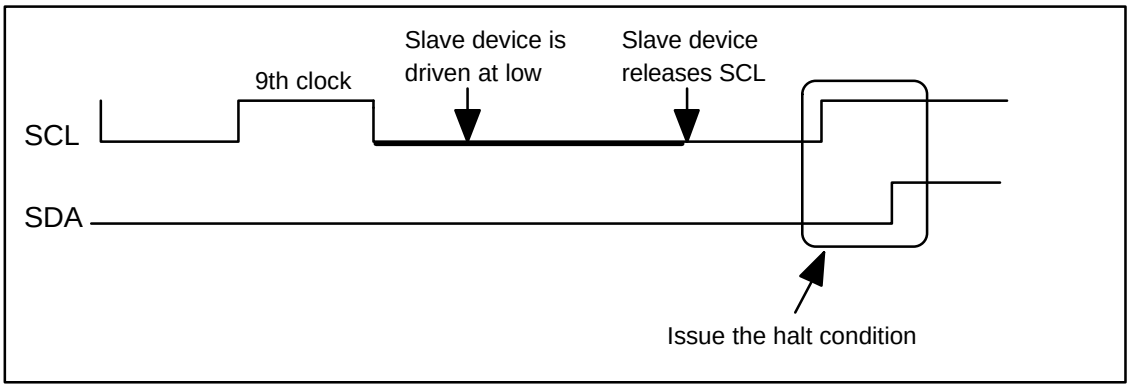


Figure 2-1 Timing for Issuing the Halt Condition

(2) Limitation on automatically switching the slave transmit mode

In slave transmit mode, set the ACKE bit (to test and select the acknowledge bit) to 1 after the falling edge of the ninth clock where the slave address has been matched.

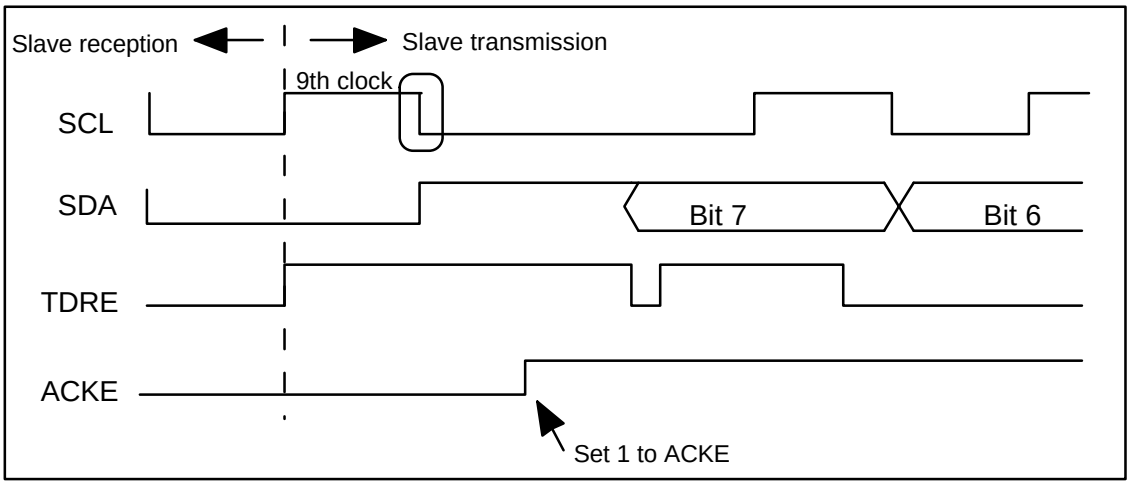


Figure 2-2 Timing for Setting ACKE

(3) Initial value of the ACKBR bit

	Initial Value of the ACKBR Bit in ICIER	Notes
Device specification	0	
Emulator specification	1	This bit is read-only.

(4) Clear condition of the IIC bus status register (ICSR)

The clear conditions for the TDRE, TEND, and RDRF flags differ.

Device specification

Bit	Bit Name	Clear Condition
7	TDRE: transmit data register empty	• When 1 is read and 0 is written • When the data is written in ICDRT
6	TEND: transmit end	
5	RDRF: receive data register full	• When 1 is read and 0 is written • When the data is written in ICDRR

Emulator specification

Bit	Bit Name	Clear Condition
7	TDRE: transmit data register empty	When 1 is read and 0 is written
6	TEND: transmit end	
5	RDRF: receive data register full	

2-2 PORT9 Register (H'FF58)

	Reads the PORT9 register.
Device specification	Reads the pin state.
Emulator specification	Reads the undefined value.

When a program is created by using the flowchart described in the H8S/2378 hardware manual, in the master transmit mode of the IIC bus format, the previous value of the MSB for the transmit data will be retained (see figure 2-3). To prevent such state, as shown in figure 2-4, transmission must be performed in each byte. Before the transmit data is written in ICDRT, test SCLO in ICCR2 and check that SCL outputs low level.

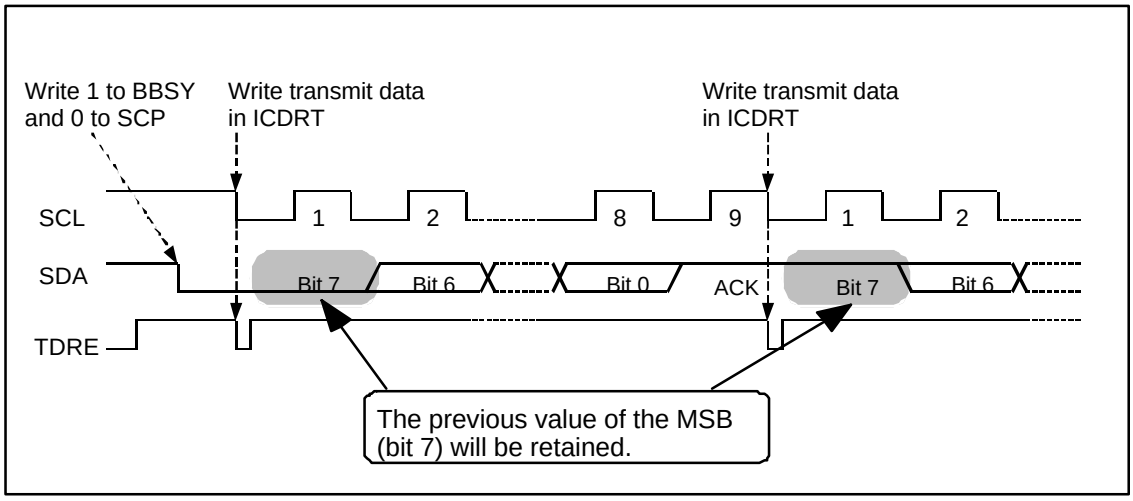


Figure 2-3 Timing when Retaining the Previous Value of MSB in the Transmit Data

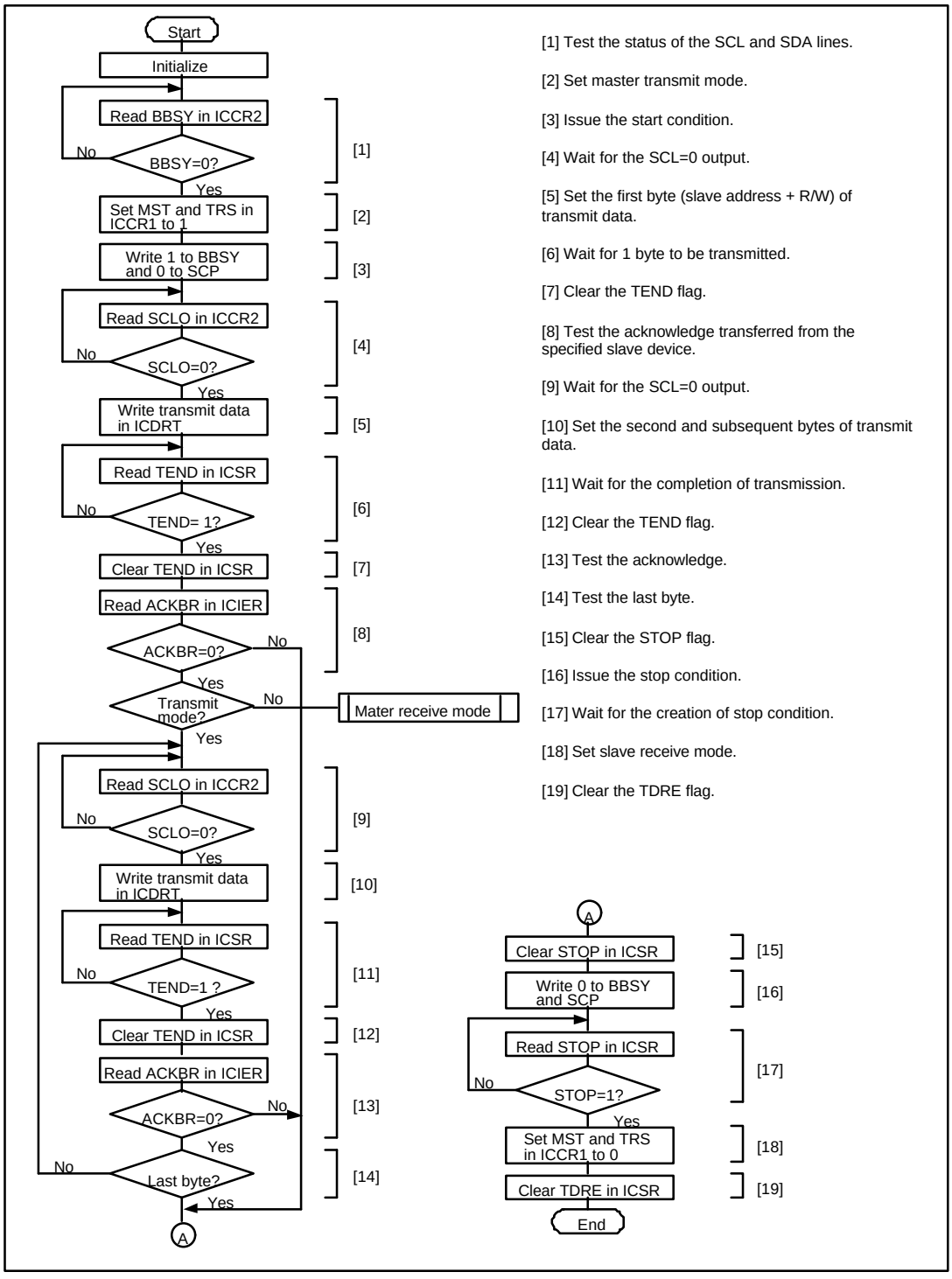


Figure 2-4 Sample Flowchart for Master Transmit Mode