To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	27 November 2001	No.	TN-EML-076A/E
THEME	Limitation on Using the H8/3664 Series, H8/3664N, H8/3672 Series, H8/3687 Series, H8/3694 Series E6000 Emulator		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	☒ Limitation on Use	
PRODUCT NAME	H8/3664 series, H8/3664N, H8/3672 series, H8/3687 series, H8/3694 series E6000 emulator Type number: HS3664EPI61H	Lot No. etc.	All lots
REFERENCE DOCUMENT	E6000 H8/3664 Series, H8/3664N, H8/3672 Series, H8/3687 Series HS3664EPI61H Supplementary Information	Effective Date From	Permanent

Thank you for using Hitachi's products.

Note that there is the following limitation on using the E6000 emulator.

1. Limitation

During program execution in the H8/3664 series, H8/3664N, H8/3672 series, H8/3687 series, H8/3694 series E6000 emulator, the program overruns when the word accessing is performed for the 8-bit internal I/O register immediately after memory operation (parallel access: display or modification in the Memory, Watch, or Disassembly window).

Note: This failure does not occur in the Bus monitor window (indicated as RAM monitor window).

2. Countermeasure:

Access the 8-bit internal I/O register in word, not in byte.

Additionally, access reading in the A/D data register in the order from upper to lower byte.

If an interrupt occurs after upper-byte accessing and the control register of the A/D converter (ADCSR/ADCR) is not modified in the interrupt processing routine, the lower data is held in the temporary register and the upper and lower data can be correctly read even if an interrupt occurs. When there is a processing that modifies ADCSR/ADCR in the interrupt processing routine, the upper and lower data cannot be correctly read. Mask the interrupt while the upper and lower data are being accessed.