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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-H8*-A434A/E	Rev.	1.00
Title	Limitation on Usage of Output State Retention by Port F		Information Category	Technical Notification		
Applicable Product	H8S/2164 Group H8S/2472, H8S/2463, H8S/2462 Group	Lot No. All lots	Reference Document	H8S/2164 Group Hardware Manual (REJ09B0429 Rev.2.00) H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual (REJ09B0403 Rev.2.00)		

We have found that the output state retention by port F in the H8S/2164 Group, and H8S/2472, H8S/2463, H8S/2462 Group, may not operate correctly in that an internal reset by the watchdog timer may change the input or output states of pins.

Therefore, we would like to inform you of the limitation on usage described below.

1. Functions to Which the Limitation Applies

Output state retention is described as follows in the parts on port F registers of section 8, I/O Ports, in the hardware manuals listed above.

(1) Port F Data Direction Register (PFDDR)

The individual bits of PFDDR specify input or output for the port F pins. PFDDR is initialized only by a system reset, and retains the value even if an internal reset signal of the WDT is generated.

(2) Port F Output Data Register (PFODR)

PFODR stores output data for the port F pins. PFODR is initialized only by a system reset, and retains the value even if an internal reset signal of the WDT is generated.

However, since we found that an internal reset generated by the watchdog timer may change the input or output states of pins, a limitation on usage of the pins of port F applies as described below.

2. Conditions that Require Limitation

(1) The possibility of an internal reset being generated by the watchdog timer

(2) A pin of port F being used as an input or output

If conditions (1) and (2) are both satisfied, the limitation described in this Technical Update is applicable.

3. Limitations on Usage

If there is a possibility of the watchdog timer generating an internal reset, pins of port F should only be used as inputs. In addition, the value of the PFODR register should not be changed from 0 (the initial state).

If the watchdog timer generates an internal reset while a pin of port F is in use as an output, the level on a pin may be changed from low to high. Moreover, at the same time when the output level is changed, the value of the PFDDR register may be changed to 0 or the value of the PFODR register may be changed to 1.