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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Date: Nov. 12, 2009

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU/MCU		Document No.	TN-SH7-A756A/E	Rev.	1.00
Title	Limitation of SH7785 PCIC Target Access and Manual Correction		Information Category	Technical Notification		
Applicable Product	SH7785 Group	Lot No. All lots	Reference Document	SH7785 Hardware Manual Rev.1.00 Jan.10.2008 (REJ09B0261-0100)		

There is a limitation about the SH7785 PCIC target access.

[Summary]

In a target write or target read transaction between the PCI local bus and the SH7785 local bus by using a memory write command or a memory read command from the PCI bus, the data may be transferred between the PCI local bus and the SH7785 local bus incorrectly. And the transaction might be terminated by the target abort termination.

It is not supported to transfer data between the PCI local bus and the SH7785 local bus with a target I/O access or a target configuration access. So this problem does not occur in a target I/O access or a target configuration access.

[Condition]

When the following conditions, (1), (2) or (3), are satisfied, the PCIC can not transfer the data between the PCI local bus and the SH7785 local bus correctly.

(1) When all the following conditions (1-a)-(1-c) are satisfied

(1-a) Target memory write access or target memory read access to SH7785 PCIC

(1-b) Using a single transaction on PCI bus

(1-c) Combination of C/BE# [3:0] signals at the data phase on the PCI bus (byte enable) are not

"LLLL/LLHH/HHLL/LHHH/HLHH/HHLH/HHHL (H: High level, L: Low level)"

(2) When all the following conditions (2-a)-(2-c) are satisfied

(2-a) Target memory write access to SH7785 PCIC

(2-b) Using a burst transaction on PCI bus

(2-c) When corresponding to one or more conditions among the following conditions (i)-(iii)

(i) Start address is not 16 byte boundary

(ii) End address is not 16 byte boundary

(iii) C/BE#[3:0] signals at the data phases on the PCI bus (byte enable) are not "LLLL" (H: High level, L: Low level)

(3) When all the following conditions (3-a)-(3-d) are satisfied

(3-a) Target memory read access to SH7785 PCIC

(3-b) Using a burst transaction on PCI bus

(3-c) Both PFE bit and PFCS bit in a PCI control register (PCICR) are set to 1.

(3-d) When corresponding to one or more conditions among the following conditions (i)-(iii)

(i) Start address is not 16 byte boundary

(ii) End address is not 16 byte boundary

(iii) C/BE# [3:0] signals at the data phase on the PCI bus (byte enable) are not “LLLL” (H: High level, L: Low level)

[Workaround]

Take one of following workarounds (1)-(4) to perform a data transfer between the PCI bus and the SH7785 local bus.

For a target read burst access, a following workaround (5) is also a workaround.

(1) Use the SH7785 DMAC for the transfer between the PCI bus and the SH7785 local bus (LBSC).

When using SH7785 DMAC, this problem does not occur.

(2) For a target access, use a single transaction, and the combination of C/BE#[3:0] at the data phase on the PCI bus must be equal to LLLL/LLHH/HHLL/LHHH/HLHH/HHLH/HHHL. (H: High level, L: Low level)

(3) For a target access, use a burst transaction, and start address and end address must be 16 byte boundary, and the combination of C/BE#[3:0] at the data phase on the PCI bus must be equal to LLLL. (All low level)

(4) The target access between the PCI bus and the DDR2-SDRAM space works correctly.

The target access between the PCI bus and the U memory space works correctly.

So transfer the data between the PCI bus and the SH7785 local space via DDR2-SDRAM space or

U memory space.

(5) For a target read burst access, PFE bit or PFCS bit in a PCI control register (PCICR) is cleared to 0.

[Manual correction]

13.4.4 Target Access

(4) Access to SH7785

Memory Space: See Section 13.4.4 (1), Accessing Memory Space in This LSI. Area 0 to 6 (CS0 – CS6) on the SH7785 memory map, DDR2-SDRAM space and U memory space in the SH4-A core can be accessed.

But it is possible that one of the following conditions (a), (b) and (c), are satisfied, when accessing area 0 to 6.

(a) For a target access, use a single transaction, and the combination of C/BE#[3:0] at the data phase on the PCI bus must be equal to LLLL/LLHH/HHLL/LHHH/HLHH/HHLH/HHHL. (H: High level, L: Low level)

(b) For a target access, use a burst transaction, and start address and end address must be 16 byte boundary, and the combination of C/BE#[3:0] at the data phase on the PCI bus must be equal to LLLL. (All low level)

(c) For a target read burst access, PFE bit or PFCS bit in a PCI control register (PCICR) is cleared to 0.

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