The limitation regarding “Clocked communication function with SPI function” in Serial Array Unit (SAU)

Precaution described below is added to the following products in the User’s Manual. These contents will be reflected at the next time of the user’s manual revision for each applicable products.

1. Details
   As for SAU use, when the slave transmission/reception function is used in “Clocked communication function that uses three lines (SCK, SI, SO) with SPI function” mode, the transmission/reception for 1 bit behave illegally before the shift clock is supplied from SCKp pin depending on asset timing of SSImn (slave select) pin.

   Note : m, n, please fit the following to the applicable product groups on this document.
   Group1: m,n=1,0   Group2: m,n=0,0

2. Conditions
   It occurs when it corresponds to all of following conditions.
   1. Slave transmission/reception function is used in “Clocked communication function that uses three lines (SCK, SI, SO) with SPI function” mode.
   2. SSImn pin is set to enable (SSEmn=1) in Serial slave select function enable register m.
   3. The shift clock phase is specified as "forward"(CKPmn=0) in Serial communication operation setting register mn (SCRmn)

3. Countermeasures
   Please correspond with either of the following countermeasures.
   - Please use shift clock phase as “reverse” (CKPmn = 1) by setting of Serial communication operation setting register mn (SCRmn).
   - Please use the communication function without SSImn pin (SSEmn = 0) by setting of Serial slave select function enable register m (SSEmn).
   - Polling the SSI signal by general purpose port, and start the communication by software.
   - Accept SSI signal by external interrupt pin, and start the communication by software.
4. Revised the contents of the User's Manual

When the user's manual revision, the following note is appended all products as a target.

"SSI\textsubscript{mn} case to be used (slave selection input), please to CKP\textsubscript{mn} bit of SCR\textsubscript{mn} register to "1" (inverting the clock phase) \((m = 0, 1, n = 0, 1)."\n
(For the purpose of common specifications in the series, it will be described in all products.)

Example of SPI Function Configuration

<Correct operation : Slave transmission/reception>

\[
\begin{align*}
\text{SCK}\textsubscript{mn} \quad \text{(CKP}\textsubscript{mn}=0) \\
\text{SI}\textsubscript{mn} \\
\text{SO}\textsubscript{mn} \\
\text{SSI}\textsubscript{mn}
\end{align*}
\]

Internal data

Communication start

Communication end

<Illegal operation : Slave transmission/reception>

\[
\begin{align*}
\text{SCK}\textsubscript{mn} \quad \text{(CKP}\textsubscript{mn}=0) \\
\text{SI}\textsubscript{mn} \quad \times
\end{align*}
\]

Internal data

\[
\begin{align*}
\text{SO}\textsubscript{mn} \\
\text{SSI}\textsubscript{mn}
\end{align*}
\]

Before SCK\textsubscript{mn} input, transmission and reception is started. Master cannot receive SQ\textsubscript{bit7}. Slave to receive bit\textsubscript{7} unintentionally.

Communication start

Communication end

Communication start

It received the eighth clock input of SCK\textsubscript{mn}, to start the next communication (transmission).

Illegal operation continues until it is SSI\textsubscript{mn} bit of SSI\textsubscript{m} register is "1" (serial-channel operation is enabled).
<table>
<thead>
<tr>
<th>Applicable Products</th>
<th>Target channel</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Group 1</strong></td>
<td></td>
</tr>
<tr>
<td>R5F10AME, R5F10AMF, R5F10AMG</td>
<td>CSI10</td>
</tr>
<tr>
<td>R5F10ALF, R5F10ALG</td>
<td></td>
</tr>
<tr>
<td>R5F10BME, R5F10BMF, R5F10BMG</td>
<td></td>
</tr>
<tr>
<td>R5F10BLC, R5F10BLD, R5F10BLE, R5F10BLF, R5F10BLG, R5F10PME, R5F10PMF</td>
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<tr>
<td>R5F10PLE, R5F10PLF</td>
<td></td>
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<tr>
<td><strong>Group 2</strong></td>
<td></td>
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<tr>
<td>R5F10PPE, R5F10PPF, R5F10PPG, R5F10PPH, R5F10PPJ</td>
<td>CSI00</td>
</tr>
<tr>
<td>R5F10PMG, R5F10PMH, R5F10PMJ</td>
<td></td>
</tr>
<tr>
<td>R5F10PLG, R5F10PLH, R5F10PLJ</td>
<td></td>
</tr>
<tr>
<td>R5F10PGG, R5F10PGH, R5F10PGJ</td>
<td></td>
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</tbody>
</table>

That is all