To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-MC*-010A/EA	Rev.	1.0
Title	Limitation of HCAN, when accessing mailbox, during HCAN sleep mode		Information Category	Usage Limitation		
Applicable Product	Stated below	Lot No. All	Reference Document	Stated below		

1. Phenomenon

When mailboxes (MDx, MCx) is accessed during HCAN sleep mode, there is a possibility that the CPU will stop. To recover from this status, either a WDT reset or an external reset is required. This phenomenon does not occur for any other mode apart than during HCAN sleep.

Furthermore, when the mailboxes are accessed when HCAN is either at halt or reset, there is no possibility of the CPU stopping.

2. Cause

In HCAN, the mailboxes (for Identifiers, data storage, etc.) are a RAM structure and this allows two-way access from both the CPU and HCAN controller. To avoid conflict in RAM accessing, the HCAN can generate a WAIT signal during preparation for CAN bus data transmitting and data receiving, this will cause a wait of CPU access to RAM (mailbox) .

The phenomenon in this report, occurs when the HCAN transfers to sleep mode while generating the WAIT signal. If the HCAN transfers to sleep mode while the WAIT signal is continuously valid, and during the sleep mode, when the CPU accesses the RAM, the WAIT signal is sent to the CPU and the CPU. This will make the CPU stay in wait state and as a result the CPU will stop.

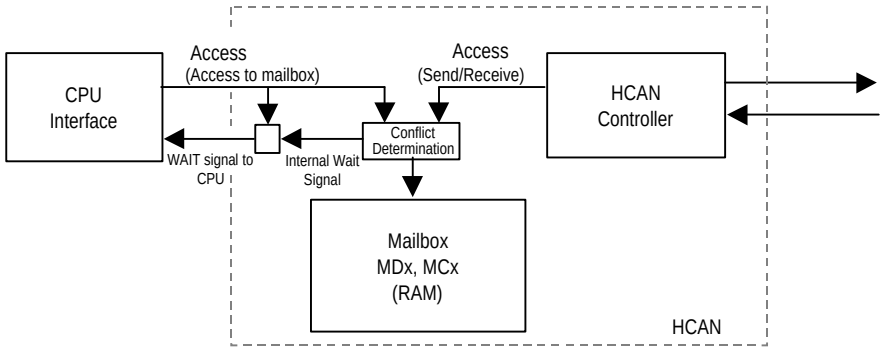

Diagram 1 HCAN RAM access conflict avoidance

3. Countermeasure

To avoid this phenomenon, please take either one of the following countermeasures.

(1) After, HCAN sleep request, do not access the mailbox (MB) until the HCAN is released from sleep mode.

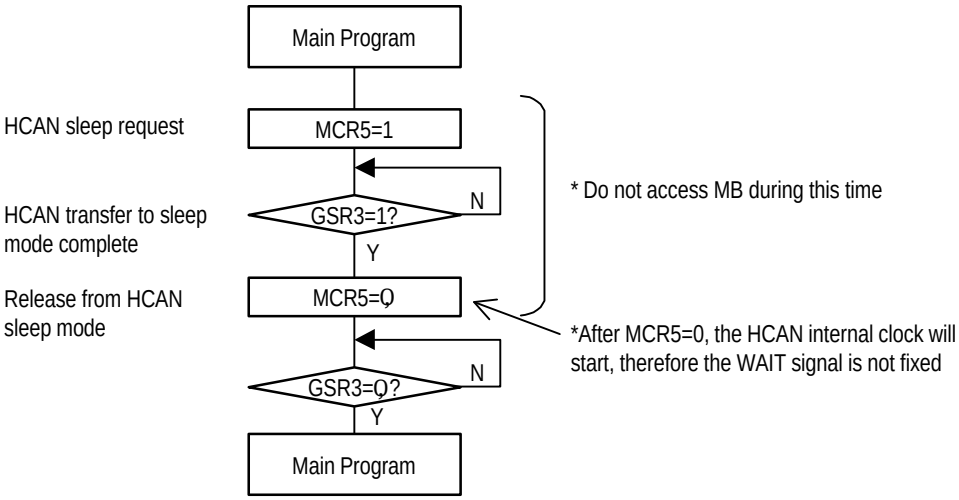

Diagram 2. Proposal flow chart using the HCAN sleep mode

(2) Instead of HCAN sleep, use either one of the following functions.

a) HCAN reset (MCR0).

b) HCAN module stop (MSTPCR). (H8S series, H8SX series, SH7047)

HCAN sleep, HCAN reset and HCAN module stop is compared in the Table 1.

Table1. HCAN Sleep, Reset, Module Stop function comparison

	HCAN Sleep	HCAN Reset	HCAN Module Stop
Control Bit	MCR5	MCR0	MSTPCR
External Send/Receive	stopped	stopped	stopped
Transfer Timing	Send/Receive: Transfer after completion of Send/Receive (at 1st bit of Intermission). During Bus Idle: Immediate Transfer		Immediate Transfer *1)
Register/RAM status	No change	REC,TEC: initialized The rest are retained	Registers: initialized MB(RAM): retained
HCAN internal clock	stopped	operational	stopped

*1) Aborted, if during Send/Receive of data (If during reception the error is detected by the other node.)

4. Supplementary Explanation

The detailed timing of this phenomenon is reported below.

Case 1: Phenomenon occurring when transmission is set during bus idle.

This phenomenon occurs when transmission is set during bus idle, and the following three conditions are met.

(1) During bus idle, the transmission is set (TXPR set), and the message is scanned.
(2) During message scan, HCAN is transferred to sleep mode.
(3) During HCAN sleep the mailboxes (MDx, MCx) is accessed.

The sequence inside HCAN is; TXPR is set, then the transmission message is scanned, then the data is stored to the transmission buffer. During this time the HCAN will generate an internal WAIT signal and when during scan the HCAN is transferred to sleep mode, the wait signal is kept as valid. After this, when the CPU accesses the mailbox, the WAIT signal is sent to the CPU and the CPU stops.

In addition, because when TXPR/TXCR set or CAN bus error is detected the scan starts in the same way, the same phenomenon as above will occur.

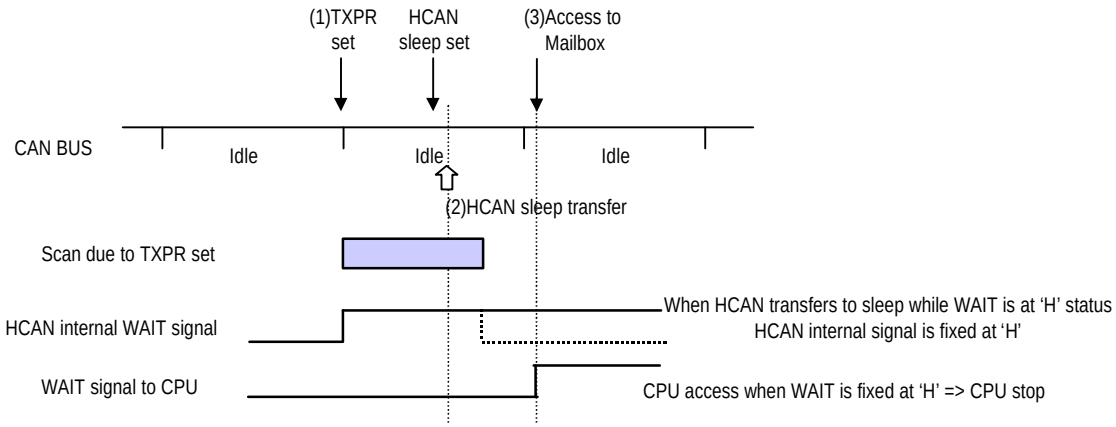

Diagram 3 Case 1 : TXPR set during bus idle

Case 2: Phenomenon occurring during reception (H8S, H8SX series)

This phenomenon occurs during reception, and the following three conditions are met.

(1) While the message is being scanned after reception completion, the mailbox is accessed.
(2) During reception scan, the HCAN is transferred to sleep mode.
(3) During HCAN sleep the mailboxes (MDx, MCx) is accessed.

The sequence inside HCAN is; When the message is received, the scan for data storage starts from the 6th bit of the EOF(End Of Frame), and normally, the scan is completed before the 1st bit of Intermission. But, if the CPU accesses the mailbox during the scan, the scan period is increased and it is possible for the scan period to go passed the 1st bit of Intermission. During this time, if the HCAN transfers to sleep mode, the wait signal will be kept as valid. After this, when the CPU accesses the mailbox, the WAIT signal is sent to the CPU and the CPU stops.

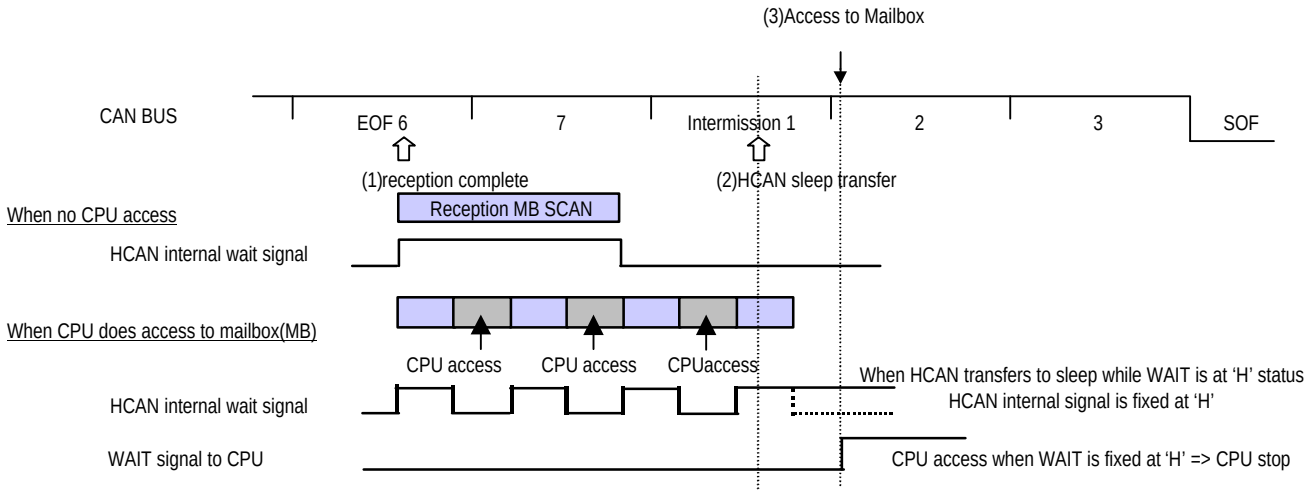

Diagram 4. Case 2 : CPU access during data reception

5. Applicable Products

Following devices have this limitation.

H8S/2282 series, H8S/2282 F-ZTAT™ hardware manual ADE-602-241

H8S/2612 series, H8S/2612 F-ZTAT™ hardware manual ADE-602-220C

H8S/2615 group hardware manual REJ09B0072-0100Z

H8S/2626 series, H8S/2623 series, H8S/2626 F-ZTAT™, H8S/2623 F-ZTAT™ hardware manual ADE-602-164C

H8S/2628 series hardware manual ADE-602-278

H8S/2636 series, H8S/2638 series, H8S/2639 series hardware manual ADE-602-189C

H8S/2646 series, H8S/2646R F-ZTAT™, H8S/2648R F-ZTAT™ hardware manual ADE-602-207C

H8S/2556, H8S/2552, H8S/2506 group hardware manual REJ09B0099-0200Z

H8SX/1520 group hardware manual REJ09B0104-0005H

SH7047 F-ZTAT™ hardware manual REJ09B0020-0100Z

SH7052, 53, 54F F-ZTAT™ hardware manual ADE-602-185B

SH7055 F-ZTAT™ hardware manual ADE-602-155C

SH7058 F-ZTAT™ hardware manual REJ09B0046-0200H

HD64404 hardware manual ADE-607-042

SH7760 hardware manual ADE-602-291