To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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RENESAS TECHNICAL UPD

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Product Category	MPU&MCU		Document No.	TN-MC*-009A/EA	Rev.	1.0
Title	Limitation on the HCAN RESET, SLEEP control bit		Information Category	Usage Limitation		
Applicable Product	See the reference documents in the following.	Lot No. All Lots	Reference Document	See the reference documents in the following		

This is a limitation discription using the HCAN.

1. Phenomenon

GSR3(bit3) of the GSR(General Status Register) will remain as “1” and the HCAN stops communication when there is a competition between “0” write of MCR0(bit0) or MCR5(bit5) of the MCR(Master Control Register) and the GSR3 set timing.

This phenomenon occurs when all of the following conditions match

1)Write “0” to MCR0/5 at the 4th clock of TSEG2 (after writing “1” to the MCR0/5 when the GSR3 is “0”).

2)GSR3’s set timing at the 5th clock of TSEG2

Diagram 1 shows an example of 2 consecutive initializations. During the 2nd initialization “1” and “0” is written to the MCR0/5 bit and the status bit GSR3 corresponds with a delay. GSR3’s clear delay timing is always fixed(1instruction to 1 bit time) but the set timing depends on the CAN bus activities. If there are no CAN bus activities the GSR3 will be set to “1” between 1 instruction to 1bit time delay, but if there are CAN bus activitiy the GSR3 set timing will be delayed maximum 1 message length. In this case the competition will occur.

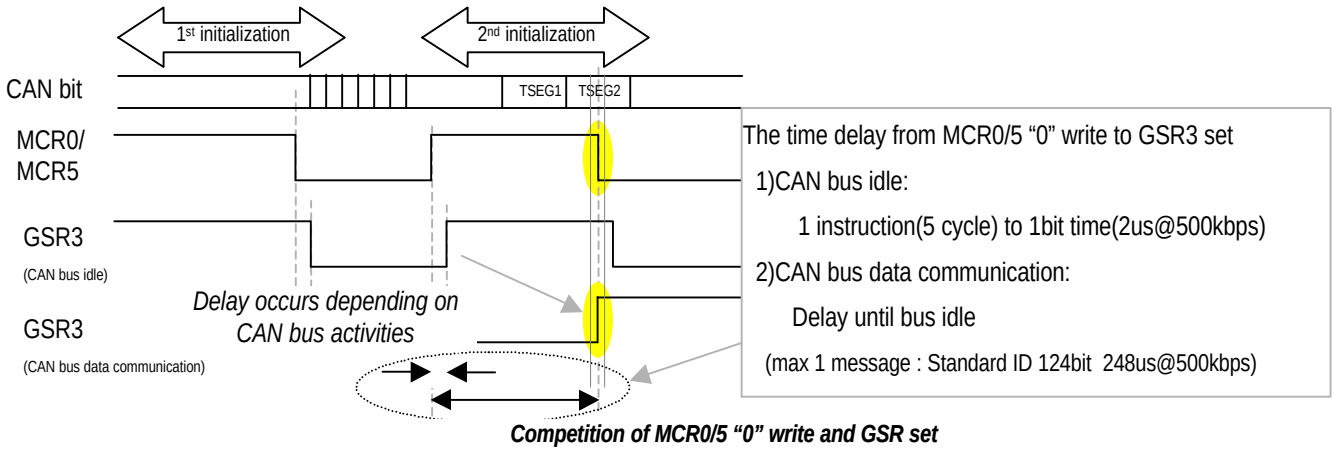

Diagram1. Timing of GSR3 stuck to 1

Detailed timings are shown in diagram 2. This limitation occurs only when the MCR0/5 “0” write signal matches the 4th clock ,GSR3 set signal matches the 5th clock of the HCAN internal clock(CP).

Furthermore, after this condition if MCR0 is written “1” and “0” the GSR3 will be cleared again and returns to the normal operating condition.

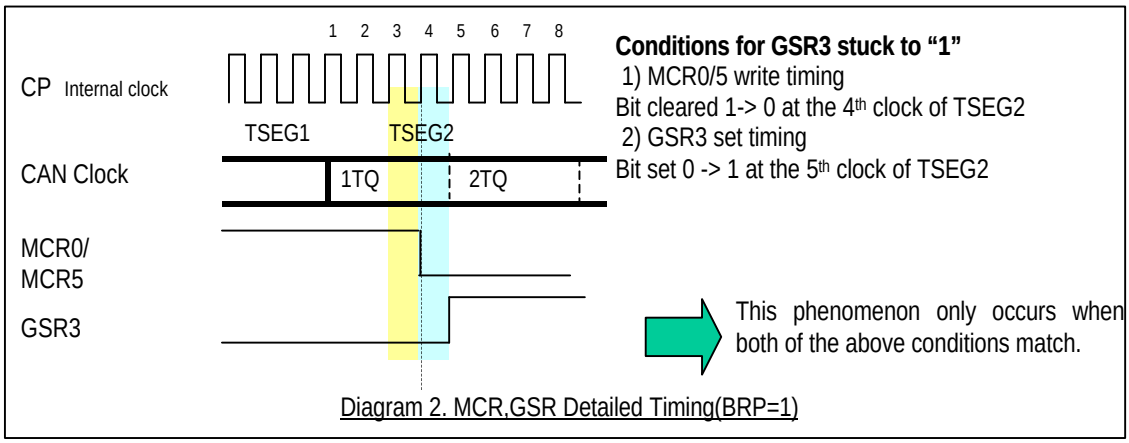

Diagram 2. MCR,GSR Detailed Timing(BRP=1)

2. Countermeasures

Please take the following countermeasures to work around this limitation.

1) Confirm that GSR3 = 1 before writing a “0” to the MCR0/5.
2) Limit the initialization proceedure to 1 time(Write 0 to MCR0/5 only once).

Note : This phenomenon will not occur at the first initialization(writing “0” to MCR0/5) after reset/module stop because the GSR3’s initial value is “1”.

3. Related devices

Following devices have this limitation.

H8S/2282 series, H8S/2282 F-ZTAT™ hardware manual	ADE-602-241 Rev 1.0
H8S/2612 series, H8S/2612 F-ZTAT™ hardware manual	ADE-602-220C Rev 4.0
H8S/2615 group hardware manual	REJ09B0072-0100Z Rev 1.0
H8S/2626 series, H8S/2623 series, H8S/2626 F-ZTAT™, H8S/2623 F-ZTAT™ hardware manual	ADE-602-164C Rev 4.0
H8S/2628 series hardware manual	ADE-602-278 Rev 1.0
H8S/2636 series, H8S/2639 series, H8S/2639 series hardware manual	ADE-602-189C Rev 4.0
H8S/2646 series, H8S/2646R F-ZTAT™, H8S/2648R F-ZTAT™ hardware manual	ADE-602-207C Rev 4.0
H8S/2556, H8S/2552, H8S/2506 group hardware manual	REJ09B0099-0200Z Rev 2.0
SH7055 F-ZTAT™ hardware manual	ADE-602-155C Rev 4.0
SH7052, 53, 54F F-ZTAT™ hardware manual	ADE-602-185B Rev 3.0