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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0082A/E	Rev.	1.00
Title	Initialization setting issue of CRU MIPI CSI2 Link Registers		Information Category	Technical Notification		
Applicable Product	RZ/G2L Group RZ/G2LC Group RZ/V2L Group	Lot No. All lots	Reference Document	RZ/G2L Group, RZ/G2LC Group User's Manual: Hardware Rev.1.00 (R01UH0914EJ0100) RZ/V2L Group User's Manual: Hardware Rev.1.00 (R01UH0936EJ0100)		

[Phenomenon]

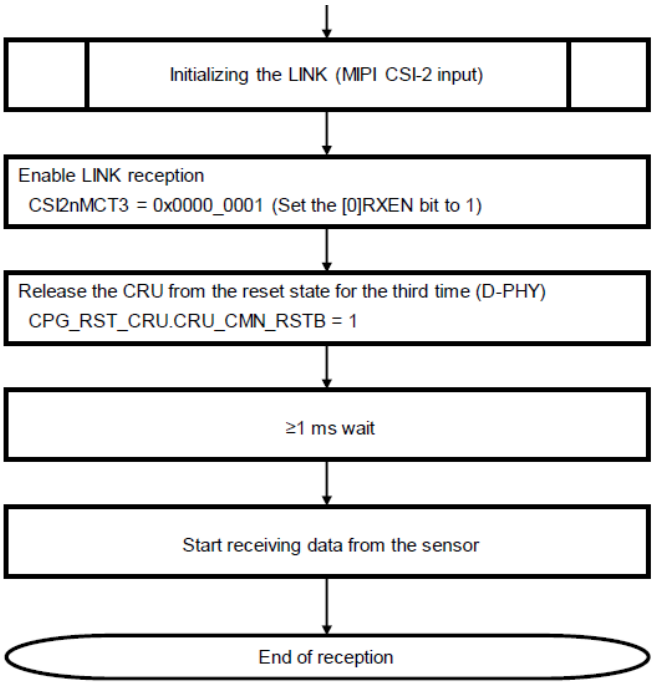
At the time of initial setting, the following MIPI-CSI2 Link register setting may not be reflected correctly.

Register Name	Abbreviation	Address
Module Control Register 0 CSI2nMCT0	CSI2nMCT0	H'0_1083_0410
Module Control Register 2	CSI2nMCT2	H'0_1083_0418
EPD Option Control Register	CSI2nEPCT	H'0_1083_0440
Receive Data Type Enable Low Register	CSI2nDTEL	H'0_1083_0460
Receive Data Type Enable High Register	CSI2nDTEH	H'0_1083_0464
Generic Short Packet Control Register	CSI2nGSCT	H'0_1083_0680

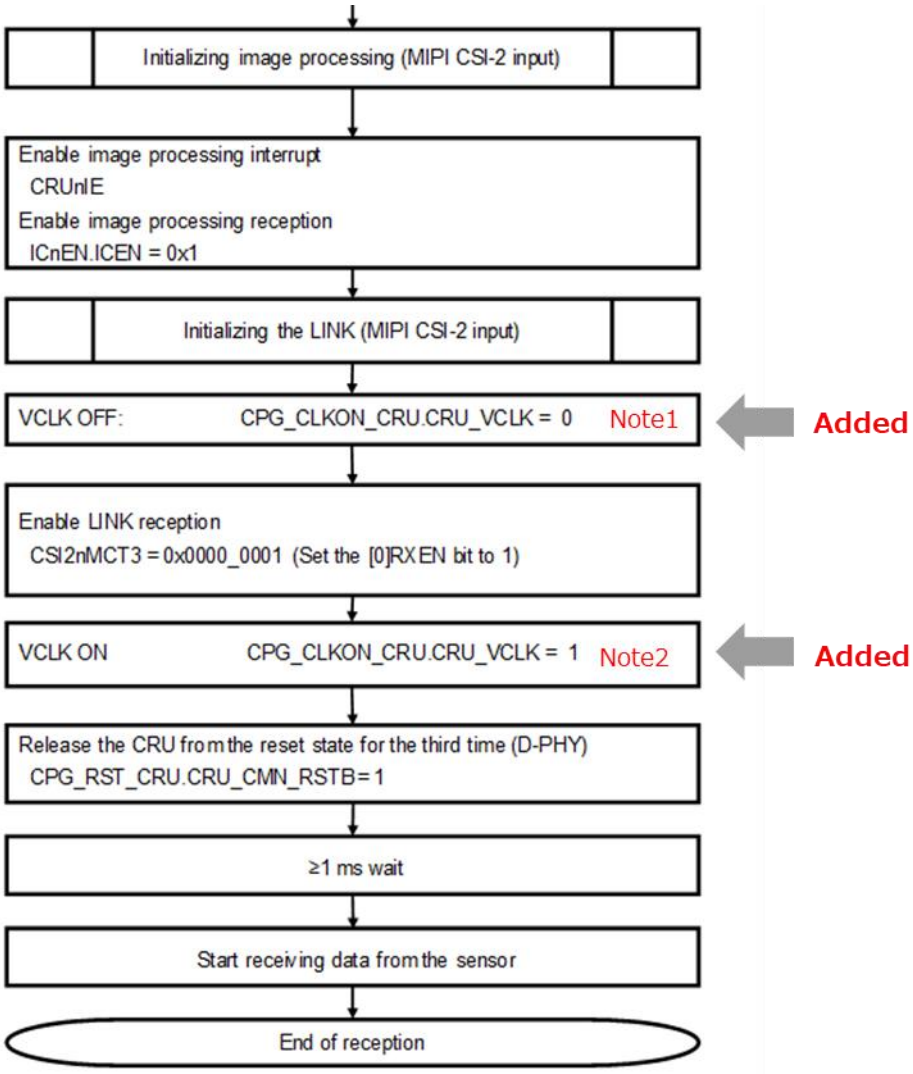
[User's Manual Update]

Additional operations are added to **"35.3.1, Figure 35.33** Reception Start Flow for the MIPI CSI-2 Input" to avoid this issue.

<Before>



<After>



Note1：After VCLK OFF setting, confirm whether VCLK is off by reading CPG_CLKMON_CRU.CLK1_ON=0.

Note2: After VCLK ON setting, confirm whether VCLK is on by reading CPG_CLKMON_CRU.CLK1_ON=1.