CUSTOMER NOTIFICATION

SUD-DT-03-0190-1-E (1/5)
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IE-789862-NS-EM1
(Control Code B)
Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-789862-NS-EM1

1. Product Version

Product name: IE-789862-NS-EM1

Control Code[Note]	Remark
A	
B	

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code	
		A	B
1	Bug in 8-bit timer/event counter 5 function	×	√
2	Bug in key-return circuit function (1)	×	√
3	Bug in key-return circuit function (2)	×	√
4	Bug in EEPROM (1)	×	√
5	Bug in EEPROM (2)	×	√
6	Addition of EEPROM illegal access condition	×	√
7	Bug in power-on-clear circuit function	×	√

×: Applicable, √: Not applicable or already corrected (addition of specification)

3. Details of Bugs and Added Specifications

No.1 Bug in 8-bit timer/event counter 5 function

[Description]

0 is read even though 1 is written to TCE5 and TMC56 of 8-bit timer/event counter 5.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.2 Bug in key-return circuit function (1)

[Description]

When the KRREN pin is low level and the mode is STOP mode, a reset can be generated at the fall of the key interrupt pin, but the KRRES flag remains 0.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.3 Bug in key-return circuit function (2)

[Description]

A non-maskable interrupt (NMI) cannot be generated by key return when the IE flag is 0.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.4 Bug in EEPROM (1)

[Description]

When the target voltage (V_{DD}) is lower than 2.7 V, access to EEPROM area 2 cannot be controlled using the EEWE pin.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.5 Bug in EEPROM (2)

[Description]

A guard break occurs when the output of 8-bit timer 80 is used as the count clock (data write time) of the EEPROM timer and EEPROM data is read while operation of 8-bit timer counter 80 is stopped.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.6 Addition of EEPROM illegal access condition

[Description]

Data can be read from the EEPROM even if read is disabled (ERE10 = 0, EWE10 = 0).

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.7 Bug in power-on-clear circuit function

[Description]

Even if 1 is written to bit 1 (POCMK1) and bit 0 (POCMK0) of the power-on-clear register (POCF), 0 is read and the operation of the POC circuit cannot be controlled.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

4. Restrictions

No.1 Reset function

[Description]

The oscillation stabilization time after reset release differs from that of the actual device.

- Actual device: 2^{12}/fx
- IE-789862-NS-EM1: 2^{17}/fx

[Workaround] There is no workaround.

No.2 Low-voltage operation

[Description]

The operating voltage range differs from that of the actual device.

- Actual device: 1.8 to 5.5 V
- IE-789862-NS-EM1: 2.0 to 5.5 V

[Workaround] There is no workaround.

No.3 EEPROM

[Description]

(1) The status differs from that of the actual device when ERE10 = 0 and EWE = 0 are set without reading/writing data from/to EEPROM.
   - Actual device: Shifts to low-current-consumption mode.
   - IE-789862-NS-EM1: Shifts to access guard (read/write disable) status.

(2) The operation differs from that of the actual device when shifting to STOP mode while data is being written.
   - Actual device: Illegal data is written.
   - IE-789862-NS-EM1: An illegal access break occurs.

(3) The operation differs from that of the actual device when read is disabled by setting bit 2 (ERE10) and bit 0 (EWE10) of EEPROM write control register 10 (EEWC10).
   - Actual device: Illegal data is read.
   - IE-789862-NS-EM1: An illegal access break occurs. (Addition of specification)

[Workaround] There are no workarounds for (1) to (3).

No.4 SFR display

[Description]

The display of the SFR window of the ID78K0S-NS (integrated debugger) is illegal because the correct value cannot be written to the 16-bit SFRs (CR00, CR01, CMD).

[Workaround]

Write values to the 16-bit SFRs (CR00, CR01, CMD) by program execution (instruction).

5. Cautions

Note the following points when using the IE-789862-NS-EM1.

(1) When emulation of the low-voltage detector and power-on-clear circuit detection voltage is performed, it is affected by voltage fluctuation and noise. Therefore, the detected voltage must be checked in the EEPROM product.

(2) When a program that illegally accesses EEPROM is executed in the IE-789862-NS-EM1, an error message is displayed and a break occurs. The conditions for illegally accessing the EEPROM and the displayed error message are described below.

Illegal Access Condition

Error message: **Unspecified Illegal**	
EEPROM illegal access conditions	
<1>	Write instruction to EEPROM is executed when EWE10 = 0.
<2>	Write instruction to EEPROM is executed while the clock selected by EEPROM (8-bit timer 80) is stopped.
<3>	Write instruction to EEPROM is executed while EEPROM is being written to.
<4>	Read instruction from EEPROM is executed while EEPROM is being written to.
<5>	Instruction is fetched from EEPROM while EEPROM is being written to.
<6>	EWE10 is set to 0 while EEPROM is being written to.
<7>	ERE10 is set to 0 while EEPROM is being written to.
<8>	Main system clock is stopped by the STOP instruction while EEPROM is being written to.
<9>	Count clock selection of the write time setting timer is changed while EEPROM is being written to.
<10>	RESET is applied while EEPROM is being written to.
<11>	Instruction is fetched from EEPROM when EWE10 = 0.
<12>	Write to EEPROM area 2 is executed when the EEWE pin is low.
<13>	Read instruction to EEPROM is executed when EWE10 = 0.
<14>	Write to EEPROM is executed when EWST = 1.

(3) The signals related to port 4 are connected to a 1 MΩ pull-up resistor in the IE-789862-NS-EM1. 3Fh is read as the initial value of port 4 under the following conditions.

(a) When the target system is not connected

(b) When all the P4 pins are left open in the target system

(4) Since bit 2 (POCOF) of the power-on-clear register (POCF) is 1 when the IE-789862-NS-EM1 is activated, set bit 2 (POCOF) to 0 in the startup routine.

(5) No error occurs even if the EEPROM write time is set to other than 3.3 to 6.6 ms.

(6) Procedure to set ERE10 and EWE10 when writing data to the EEPROM

(a) Set ERE10 = 1

(b) Set EWE10 = 1

(c) Insert a wait for 1 ms or longer using software.

(d) The program shifts to the EEPROM write state

No error occurs even if the wait in (c) is less than 1 ms.