CUSTOMER NOTIFICATION

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IE-789488-NS-EM1

Preliminary User's Manual

2nd edition, July 2001

Major Revisions in 2nd Edition

Page	Description
pp. 3, 8, 11, 21, 22, 26, 27, 29	Addition of description on IE-78K0S-NS-A (main board on main unit)
pp. 5 to 7	Addition of 2.2 Initial Settings of Switches and Jumpers Modification of section order in CHAPTER 3 INSTALLATION Addition of 3.2 Settings of Switches and Jumpers on Main Board 3.6 Settings of Subsystem Clock x4 Circuit Addition of figures Figure 2-2 Names of Parts on I/O Board (IE-789488-NS-EM1 I/O Board) Figure 3-3 Outline of System Clock Figure 3-9 When Using Clock Already Mounted on Emulation Board (Subsystem Clock) Figure 3-10 When Using Clock Mounted by User (Subsystem Clock) Figure 3-13 When Using External Clock (Subsystem Clock) Figure 3-14 Mask Option Setting of Port 5 Figure 4-4 Equivalent Circuit of Emulation Circuit (4) Addition of tables Table 2-1 Initial Settings of Switches and Jumpers Table 3-1 Setting of Switches and Jumpers on IE-78K0S-NS Table 3-2 Setting of Switches and Jumpers on IE-78K0S-NS-A Table 3-5 Isolation Setting of VSS and AVSS Table 3-9 Subsystem Clock x4 Circuit Settings
pp. 8, 12	Correction of erroneous description
p. 10	Addition of conversion socket and adapter products
p. 13	Correction of erroneous description Deletion of J1 to J8
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pp. 41 to 45	Correction of erroneous description Modification of section order Deletion of J1 to J8
p. 46	Correction of erroneous description
p. 48	Addition of APPENDIX B CAUTIONS ON TARGET SYSTEM DESIGN

INTRODUCTION

Product Overview

The IE-789488-NS-EM1 is designed to be used with the IE-78K0S-NS or IE-78K0S-NS-A to debug the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

- μPD789477 Subseries: μPD78F9478, 789477
- μPD789488 Subseries: μPD78F9488, 789488

Target Readers

This manual is intended for engineers who will use the IE-789488-NS-EM1 with the IE-78K0S-NS or IE-78K0S-NS-A to perform system debugging.
Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization

When using the IE-789488-NS-EM1, refer to not only this manual (supplied with the IE-789488-NS-EM1) but also the manual that is supplied with the IE-78K0S-NS or IE-78K0S-NS-A.

IE-78K0S-NS User's Manual	IE-78K0S-NS-A User's Manual	IE-789488-NS-EM1 User's Manual
• Basic specifications • System configuration • External interface functions	• Basic specifications • System configuration • External interface functions	• General • Part names • Installation • Differences between target devices and target interface circuits • Cautions

Purpose

This manual's purpose is to explain various debugging functions that can be performed when using the IE-789488-NS-EM1.

Terminology The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is the device (a real chip) that is the target for emulation.
Target system	This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K0S-NS or IE-78K0S-NS-A and the IE-789488-NS-EM1.

Conventions

Data significance: Higher digits on the left and lower digits on the right

Note: Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

Remark: Supplementary information

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LIST OF TABLES

CHAPTER 1 GENERAL

The IE-789488-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

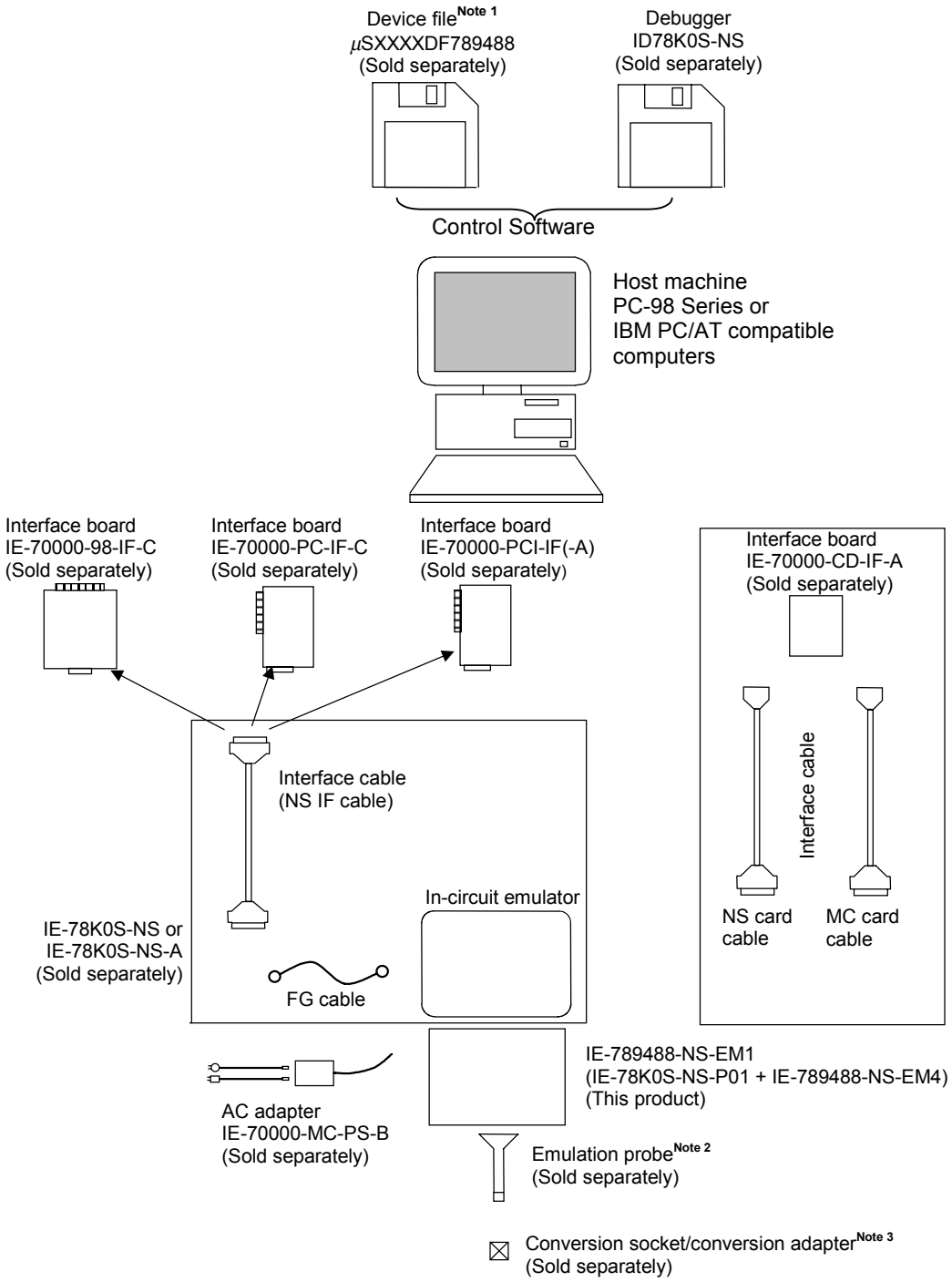
This chapter describes the IE-789488-NS-EM1 system configuration and basic specifications.

- Target device
  - μPD789477 Subseries
  - μPD789488 Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-789488-NS-EM1 system configuration.

Figure 1-1. System Configuration



Notes 1. The device file is as follows.

μSXXXXDF789488: μPD789477, 789488 Subseries

2. The emulation probe is as follows.

NP-80GC: 80-pin plastic QFP (probe length: 200 mm)

NP-80GC-TQ: 80-pin plastic QFP (probe length: 200 mm)

NP-H80GC-TQ: 80-pin plastic QFP (probe length: 400 mm)

NP-80GK: 80-pin plastic TQFP (probe length: 200 mm)

NP-80GK-TQ: 80-pin plastic TQFP (probe length: 400 mm)

NP-80GC, NP-80GC-TQ, NP-H80GC-TQ, NP-80GK, and NP-80GK-TQ are products of Naito Densei Machida Mfg. Co., Ltd.

Contact: Naito Densei Machida Mfg. Co., Ltd. (TEL: 045-475-4191)

3. The conversion socket and conversion adapter are as follows.

EV-9200GC-80: 80-pin plastic QFP (GC-8BT)

TGC-080SBP: 80-pin plastic QFP (GC-8BT)

TGK-080SDP: 80-pin plastic TQFP (GK-9EU)

TGC-080SBP and TGK-080SDP are products of Tokyo Eletech Corporation.

For further information, contact: Daimaru Kogyo, Ltd.

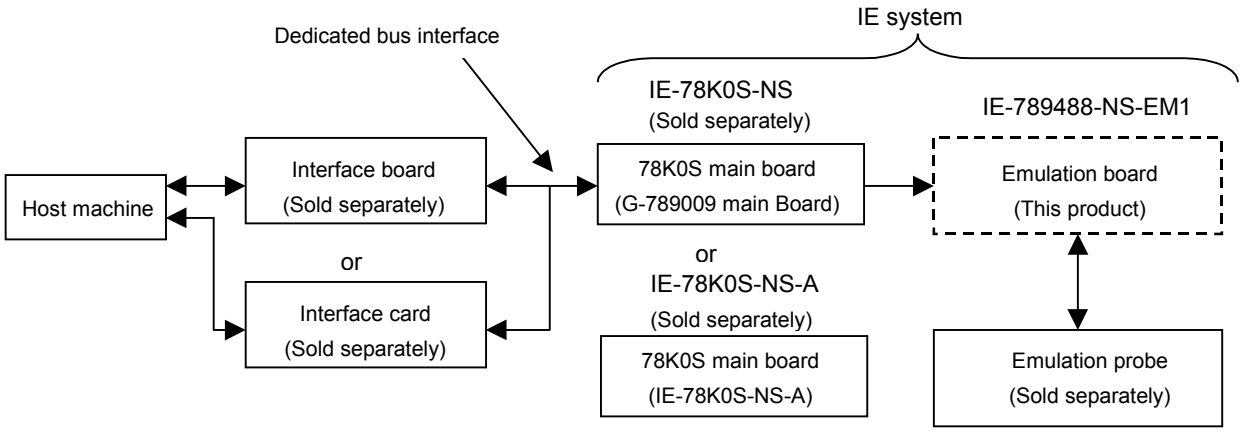
Tokyo Electronics Department (TEL +81-3-3820-7112)

Osaka Electronics Department (TEL +81-6-6244-6672)

1.2 Hardware Configuration

Figure 1-2 shows the IE-789488-NS-EM1's position in the basic hardware configuration.

Figure 1-2. Basic Hardware Configuration



1.3 Basic Specifications

The IE-789488-NS-EM1's basic specifications are listed in Table 1-1.

Table 1-1. Basic Specifications

Parameter	Description
Target device	μPD789477, 789488 Subseries
System clock	Main system clock: 1.000 to 5.000 MHz Subsystem clock: 32.768 kHz
Main clock supply	Internal: Mounted on the emulation board (5.000 MHz) or mounted by user on the parts board External: Pulse input from the target system via an emulation probe
Subclock supply	Internal: Mounted on the emulation board (32.768 kHz) or mounted by user on the parts board External: Pulse input from the target system via an emulation probe
Target interface voltage	VDD = 1.8 V to 5.5 V: Same as the target device When target system not connected: Operates @ 5 V internal voltage

CHAPTER 2 PART NAMES

This chapter introduces the parts of the IE-789488-NS-EM1 main unit.

The packing box contains the emulation board (IE-789488-NS-EM1), package details, user's manual, and guarantee card.

If there are any missing or damaged items, please contact an NEC sales representative.

Fill out and return the guarantee card that comes with the main unit.

2.1 Names of Parts on Board

The IE-789488-NS-EM1 includes the following two boards.

- Probe board (IE-789488-NS-EM1 PROBE Board): 1
- I/O board (IE-789488-NS-EM1 I/O Board): 1

Figure 2-1 shows the names of the parts on the probe board.

Figure 2-1. Names of Parts on Probe Board (IE-789488-NS-EM1 PROBE Board)

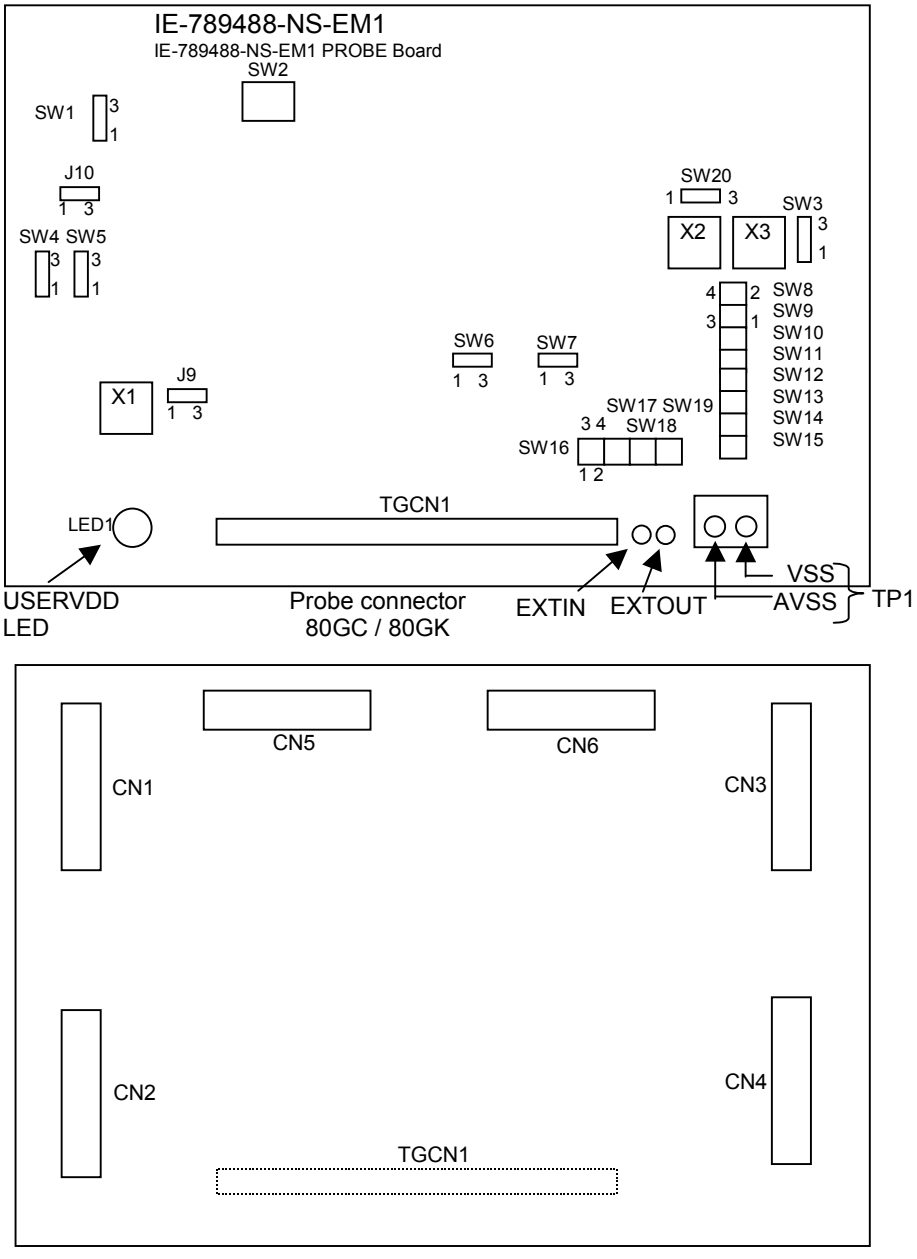
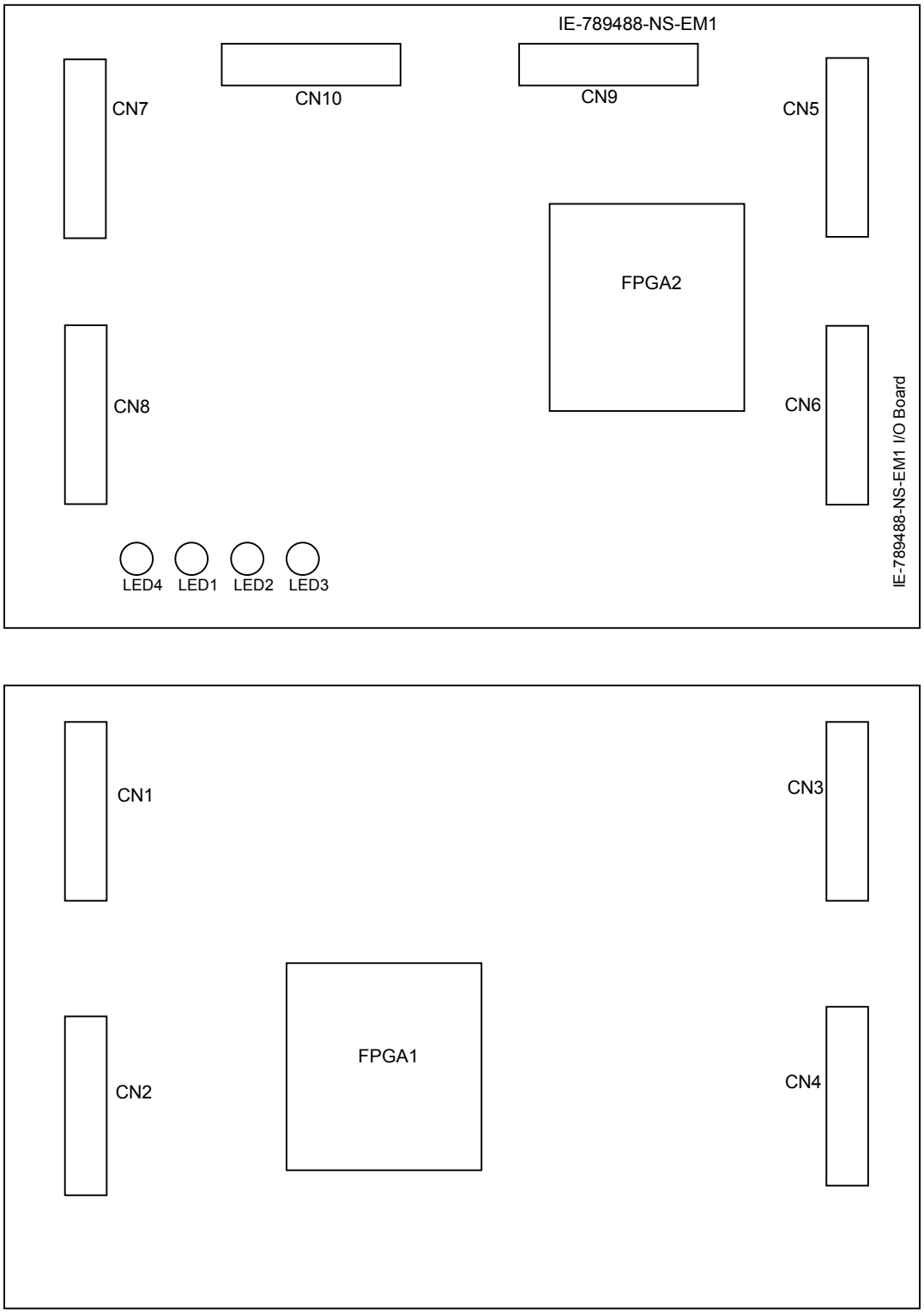


Figure 2-2 shows the names of the parts on the I/O board.

Figure 2-2. Names of Parts on I/O Board (IE-789488-NS-EM1 I/O Board)



2.2 Initial Settings of Switches and Jumpers

Table 2-1 shows the initial settings of jumpers and switches on the IE-789488-NS-EM1 probe board (IE-789488-NS-EM1 PROBE Board).

Refer to **3.3 Switch and Jumper Settings** for the J9, SW4, and SW6 settings.

Refer to **3.5 Clock Settings** for the SW1 setting.

Refer to **3.6 Subsystem Clock x4 Circuit Settings** for the SW3 and SW20 settings.

Refer to **3.7 Mask Option Settings** for the SW2, SW8 to SW19 settings.

Use SW5, SW7, and J10 with the default settings.

Table 2-1. Initial Settings of Switches and Jumpers

	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10
Initial setting	2-3	All OFF	1-2	1-2	1-2	1-2	2-3	1-3 2-4	1-3 2-4	1-3 2-4
	SW11	SW12	SW13	SW14	SW15	SW16	SW17	SW18	SW19	SW20
Initial setting	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	1-3 2-4	2-3
	J9	J10								
Initial setting	1-2	1-2								

There are no jumpers and switches on the I/O Board (IE-789488-NS-EM1 I/O Board).

CHAPTER 3 INSTALLATION

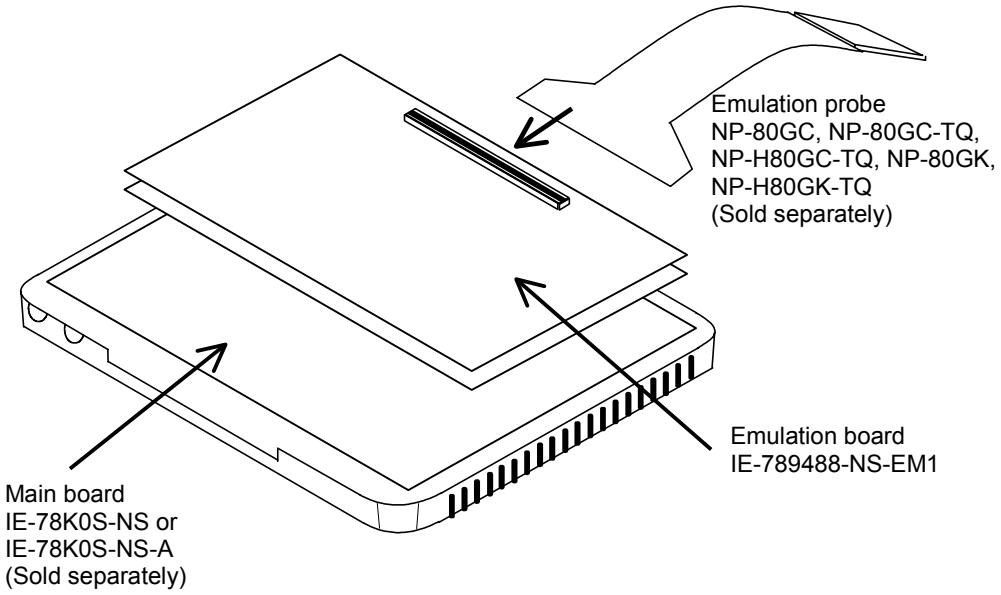
This chapter describes methods for connecting the IE-789488-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A and emulation probe. Mode setting methods are also described.

Caution Connecting or removing parts to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched off.

3.1 Connection

A connection diagram of the emulation probe and the main board is shown in Figure 3-1.

Figure 3-1. Mounting of Emulation Probe



(1) Connection with IE-78K0S-NS or IE-78K0S-NS-A main unit

See the IE-78K0S-NS or IE-78K0S-NS-A User's Manual for a description of how to connect the IE-789488-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A.

(2) Connection with emulation probe

See the IE-78K0S-NS or IE-78K0S-NS-A User's Manual for a description of how to connect an emulation probe to the IE-789488-NS-EM1.

On this board, connect the emulation probe to TGCN1.

Caution Incorrect connection may damage the IE system. For more details on connection, see the user's manual for each emulation probe.

3.2 Settings of Switches and Jumpers on Main Board

(1) Setting of IE-78K0S-NS

Before using the IE-789488-NS-EM1, set each jumper and switch as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS User's Manual.

Table 3-1. Setting of Switches and Jumpers on IE-78K0S-NS

	SW1	SW3	SW4	JP1	JP4
Setting	OFF	All "ON"	All "ON"	2-3	1-2

Caution Be sure to set the switches and jumpers as described above; otherwise the IE-78K0S-NS may be damaged.

(2) Setting of IE-78K0S-NS-A

Before using the IE-789488-NS-EM1, set each jumper and switch as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS-A User's Manual.

Table 3-2. Setting of Switches and Jumpers on IE-78K0S-NS-A

	SW1	JP1	JP3
Setting	OFF	1-2	Shorted (fixed)

Caution Be sure to set the switches and jumpers as described above; otherwise the IE-78K0S-NS may be damaged.

3.3 Settings of Switches and Jumpers

3.3.1 Jumper setting for selecting subseries

With the IE-789488-NS-EM1, a jumper setting can be used to select which subseries, the μPD789477 Subseries or the μPD789488 Subseries, will be debugged. By default, the μPD789477 Subseries is selected.

The connection setting for the jumper is shown in Table 3-3.

Table 3-3. Jumper Setting to Select Subseries

Subseries Selection	J9 Setting
μPD789477 Subseries	1-2 shorted (default)
μPD789488 Subseries	2-3 shorted

Caution Set the jumper when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

3.3.2 LCD emulation setting for μPD789488 Subseries

In the IE-789488-NS-EM1, the panel voltage (power supply of the target system) is set by switching the internal power supply between 5 V and 3 V using SW4, not by setting the boost voltage in the LCD display mode register. Refer to **CHAPTER 5 CAUTIONS** for differences between the target device and target interface circuit settings.

The connection settings for 5 V and 3 V are shown in Table 3-4.

Table 3-4. LCD Panel Voltage Setting

Panel Voltage Setting	SW4 Setting
Connected to internal power supply 5 V	1-2 (default)
Connected to internal power supply 3 V	2-3

Cautions 1. Set SW4 when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

2. The voltage set to SW4 is always used as the panel voltage regardless of the setting of bit 0 (GAIN) of LCD boost voltage control register 0 (LCDVA0).

3.3.3 Isolation setting for digital/analog ground

In the IE-789488-NS-EM1, the digital and analog ground can be isolated by a switch.

By default, VSS and AVSS are connected via a filter.

The setting of the switch is shown in Table 3-5.

Table 3-5. Isolation Setting of VSS and AVSS

Status	SW6 Setting
VSS and AVSS are connected via a filter.	1-2 shorted (default)
VSS and AVSS are isolated.	2-3 shorted

Cautions 1. Set SW6 when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

2. Be sure to use the 1-2 shorted setting when the target system is not connected.

3.4 Settings of Target Interface Voltage

Because the IE-789488-NS-EM1 internally generates the voltage for the target interface (1.8 to 5.5 V; the same as the voltage to the device) supplied from the VDD pin of the emulation probe, no special setting is necessary.
When the target system is used, be sure to supply the same voltage as the target system to the VDD pin.
When the target system is not used (VDD = 0 V), the emulator is designed to automatically operate on the internal voltage (5 V).
The settings for the target interface voltage are shown in Table 3-6.

Table 3-6. Target Interface Voltage Settings

Target Interface Voltage		Integrated Debugger (ID78K0S-NS) Operation Voltage Selection
When the target system is used	1.8 to 5.5 V	Target
When the target system is not used	5 V	Internal

Cautions 1. When using the target system, open the configuration dialog box when starting the integrated debugger and select "Target" in the operation voltage selection area (Voltage).

2. The maximum current that can be consumed when operating on VDD current of the target is 1.8 to 5.5 V: approx.100 mA.

3. The TP1 GND pin can be connected to VSS and AVSS on the pin board to reinforce GND. VSS and AVSS of the target system can be independently supplied to the in-circuit emulator.

3.5 Clock Settings

3.5.1 Outline of clock settings

The system clock to be used during debugging can be selected from (1) to (3) below.

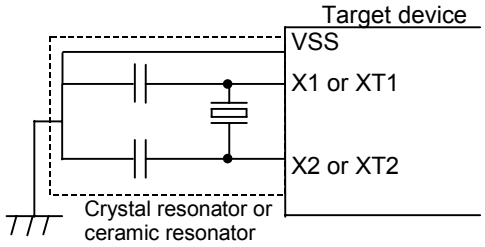
(1) Clock already mounted on emulation board
(2) Clock mounted by user
(3) External clock

"(3) External clock" can be selected only when the target system shown in part (b) of Figure 3-2 includes an external clock. If the target system shown in part (a) of Figure 3-2 includes a clock oscillator, select "(1) Clock already mounted on emulation board" or "(2) Clock mounted by user".

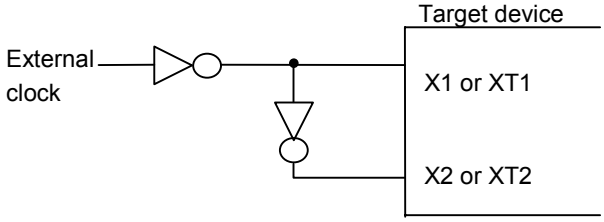
The pin connected to X2 or XT2 is not used in the IE-789488-NS-EM1.

Figure 3-2. External Circuits Used as System Clock Oscillator

(a) Internal clock



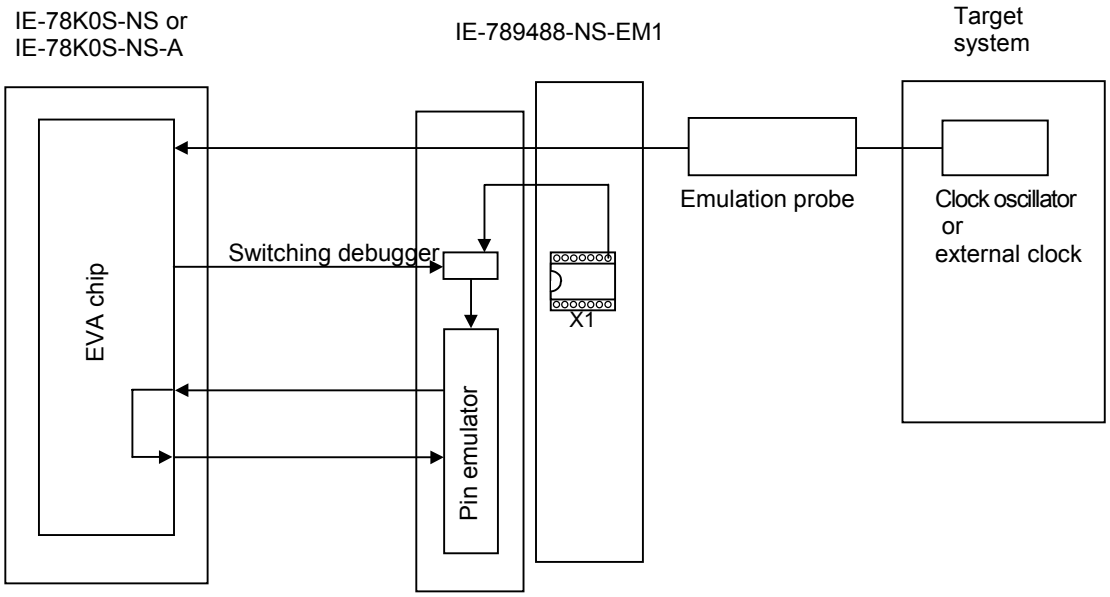
(b) External clock



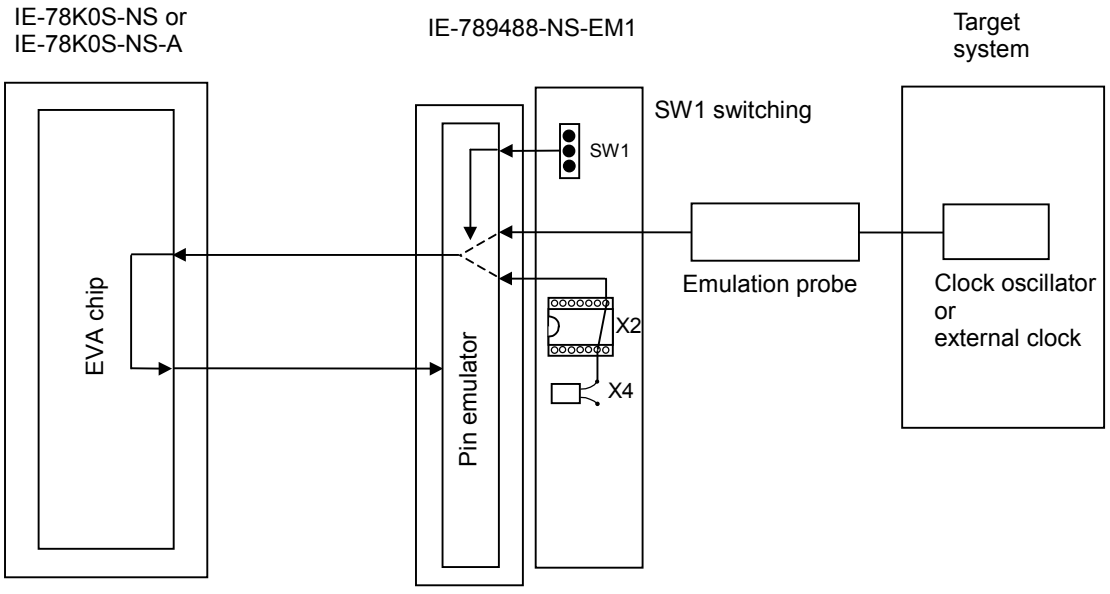
An outline of the system clock is shown in Figure 3-3.

Figure 3-3. Outline of System Clock

(a) Main system clock



(b) Subsystem clock



3.5.2 Main system clock settings

The settings of the main system clock are shown in Table 3-7.

Table 3-7. Main System Clock Settings

Frequency of Main System Clock		IE-789488-NS-EM1	Integrated Debugger (ID78K0S-NS)
		Parts Board (X2)	CPU Clock Source Selection
(1) Clock already mounted on emulation board	5.000 MHz	Oscillator	Internal
(2) Clock mounted by user	1.000 to 5.000 MHz	Oscillator or oscillator circuit assembled by user	
(3) External clock		Oscillator not used	Internal

The IE-789488-NS-EM1's factory settings are those listed above under "when using clock already mounted on emulation board".

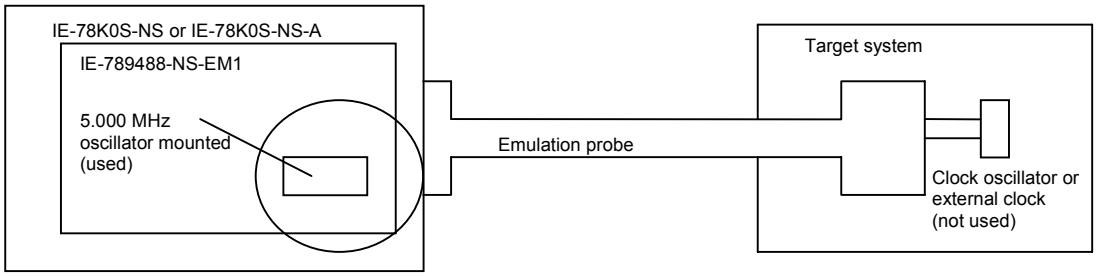
The main system clock settings of (1) to (3) are individually described in the following pages.

(1) When using clock already mounted on emulation board

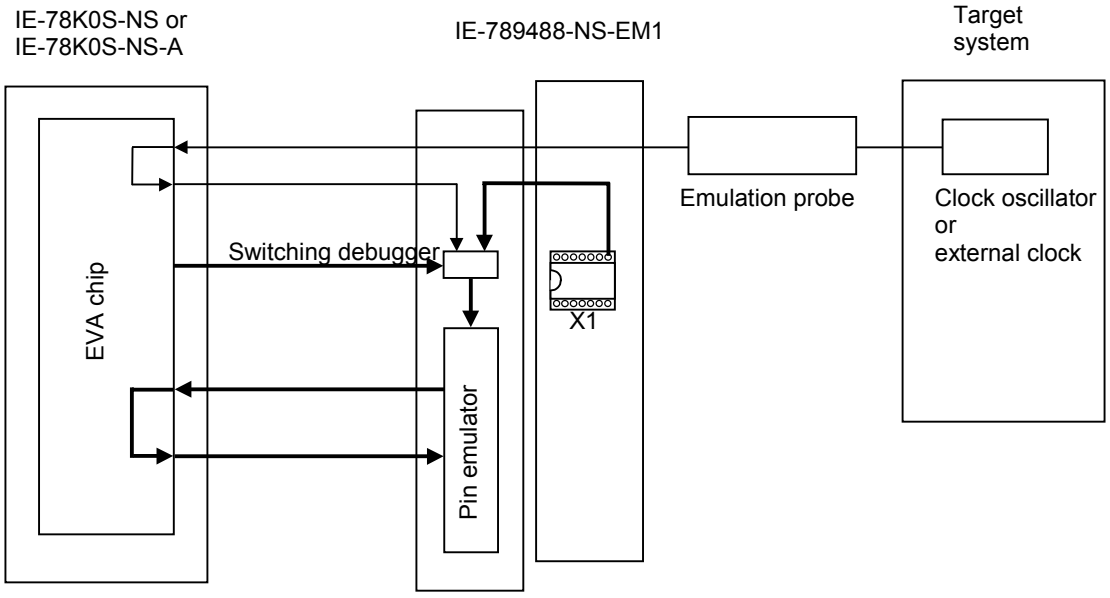
When the IE-789488-NS-EM1 is shipped, a 5.000 MHz crystal oscillator is already mounted in the IE-789488-NS-EM1's X1 socket. When using the factory-set mode settings, there is no need to make any other hardware settings.

A setting outline is shown in Figure 3-4. When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).

Figure 3-4. When Using Clock Already Mounted on Emulation Board (Main System Clock)



Remark The clock that is supplied by the IE-789488-NS-EM1's oscillator (encircled in the figure) is used.



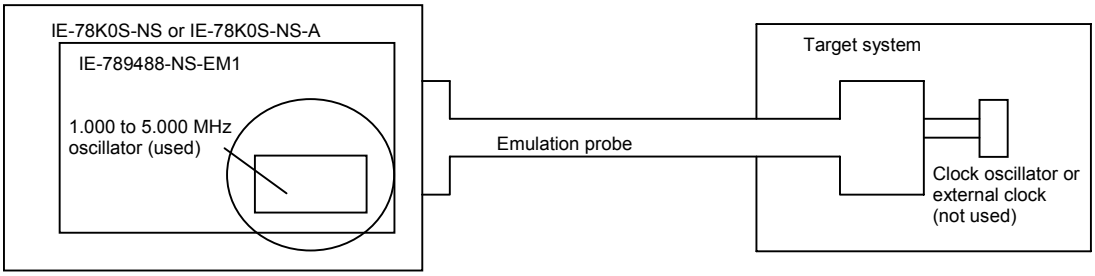
Remark The flow of the clock is indicated by the bold line.

(2) When using clock mounted by user

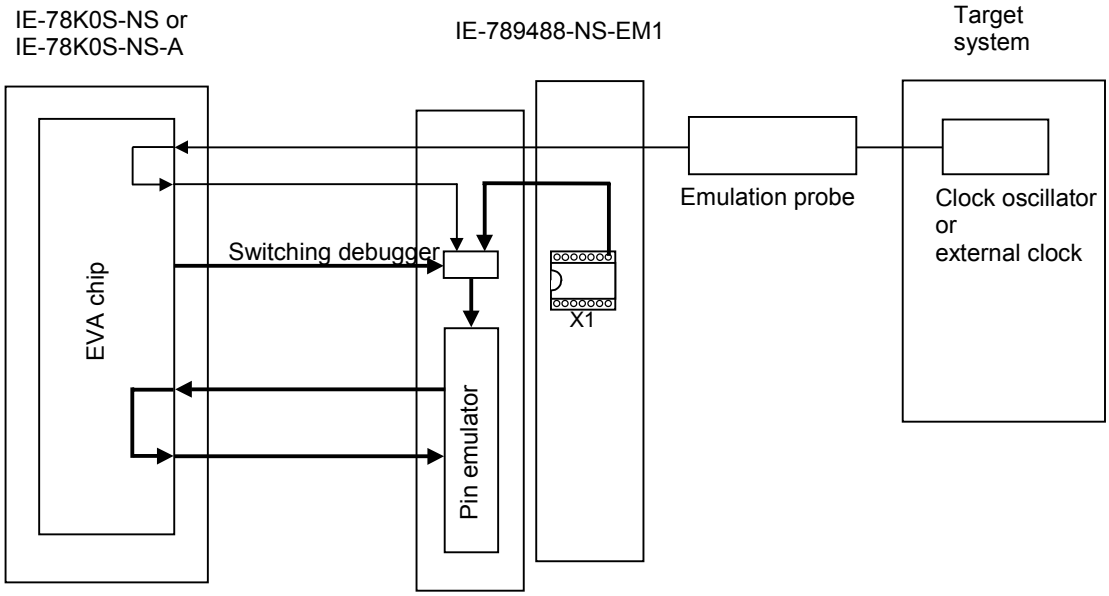
Remove the crystal oscillator already mounted on the emulation board (X1: 5.000 MHz) and mount the parts board (oscillator) that includes the oscillator or resonator to be used. This is effective when debugging with a clock with a different frequency from the clock already mounted (1.000 MHz to 5.000 MHz).

A setting outline is shown in Figure 3-5. The settings of either (a) or (b) described in the following pages are required, depending on the type of clock to be used. When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select “Internal” in the area (Clock) for selecting the CPU’s clock source (this selects the emulator’s internal clock).

Figure 3-5. When Using Clock Mounted by User (Main System Clock)



Remark The clock that is supplied by the IE-789488-NS-EM1’s oscillator (encircled in the figure) is used.



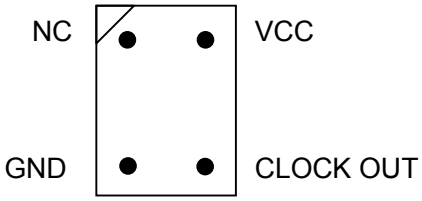
Remark The flow of the clock is indicated by the bold line.

(a) When using a crystal oscillator

♦ Necessary items

• Crystal oscillator (with pin configuration as shown in Figure 3-6)

Figure 3-6. Crystal Oscillator (Main System Clock)

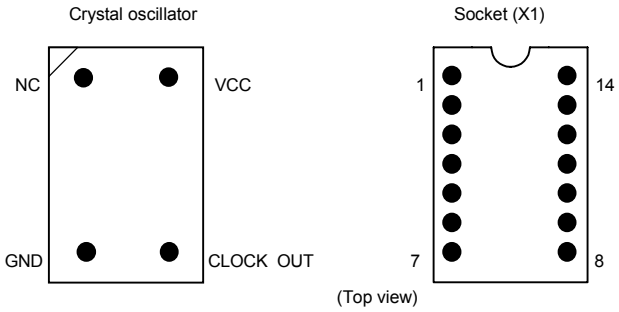


<Procedure>

<1> Prepare the IE-789488-NS-EM1.

<2> Remove the crystal oscillator from the socket (marked X1) on the IE-789488-NS-EM1.

<3> Mount the new crystal oscillator in the socket (X1) from which the oscillator was removed in <2>above. At this time, insert the oscillator into the socket aligning the pins as indicated below.



Crystal Oscillator Pin	Socket Pin No.
NC	1
GND	4
CLOCK OUT	8
VCC	14

<4> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

Caution Remove and solder the oscillator on the board when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

(b) When using a ceramic or crystal resonator

♦ Necessary items

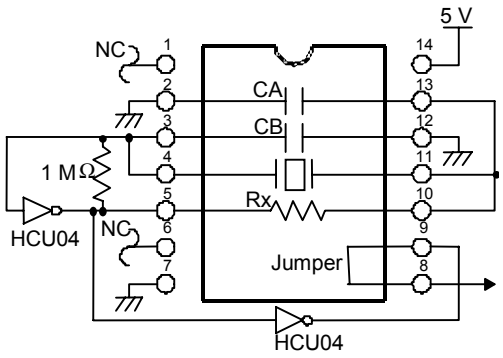
- Parts board
- Ceramic or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Solder kit

<Procedure>

<1> Solder the target ceramic or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board (as shown below).

Figure 3-7. Connections on Parts Board (Main System Clock)

Parts board (X1)



Pin No.	Connection
2-13	Capacitor CA
3-12	Capacitor CB
4-11	Resonators
5-10	Resistor Rx
8-9	Shorted

Remark NC: No Connection

<2> Prepare the IE-789488-NS-EM1.

<3> Remove the crystal oscillator that is mounted in the IE-789488-NS-EM1's socket (marked X1).

<4> Connect the parts board (from <1> above) to the socket (X1) from which the crystal oscillator was removed. Check the pin 1 mark to make sure the board is mounted in the correct direction.

<5> Make sure that the parts board mounted in the X1 socket on the emulation board is wired as shown in Figure 3-7 above.

<6> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

Caution Remove and solder the oscillator on the board when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

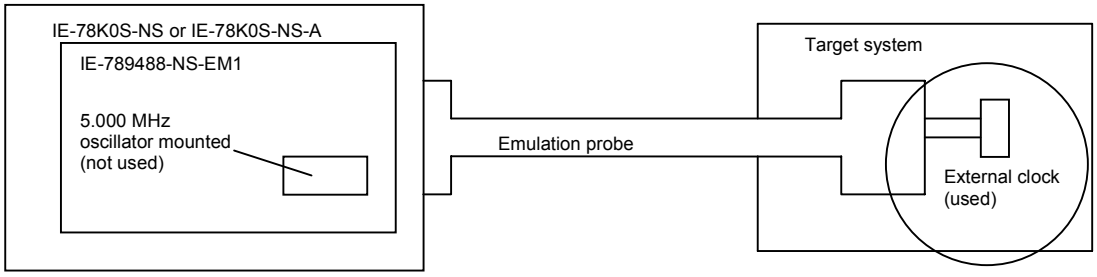
(3) When using an external clock

The external clock pulse signal on the target system is used via an emulation probe. There is no need to make any other hardware settings.

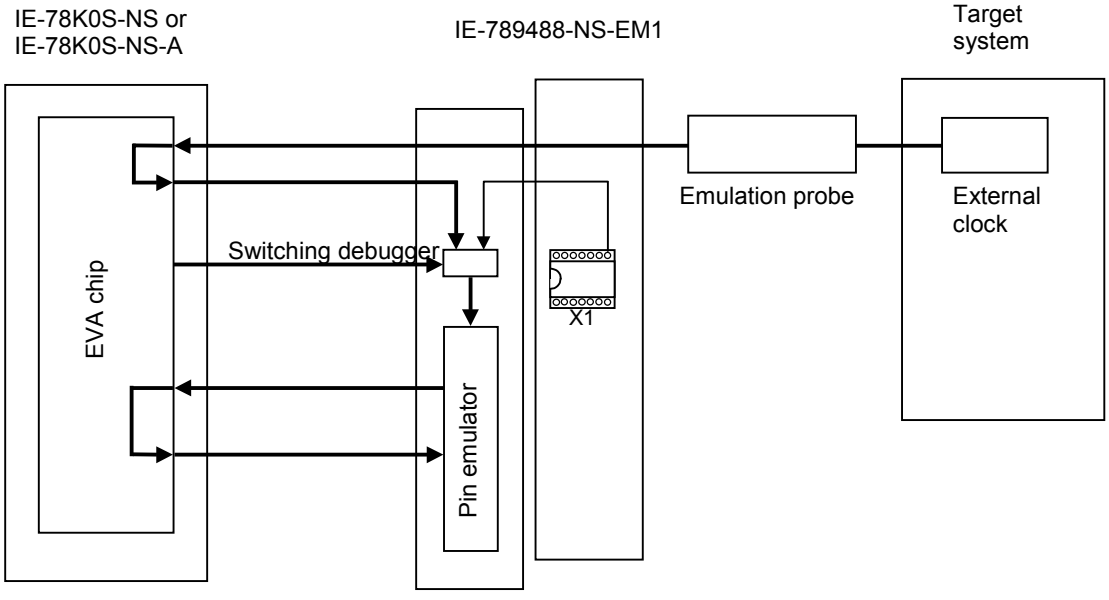
A setting outline is shown in Figure 3-8. When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select “External” in the area (Clock) for selecting the CPU’s clock source (this selects the user clock).

Caution The clock input from the target should be a rectangular wave.

Figure 3-8. When Using External Clock (Main System Clock)



Remark The clock that is supplied by the target system’s clock oscillator or an external clock (encircled in the figure) is used.



Remark The flow of the clock is indicated by the bold line.

3.5.3 Subsystem clock settings

The settings of the subsystem clock are shown in Table 3-8.

Table 3-8. Subsystem Clock Settings

Frequency of Subsystem Clock When Subclock (SCT) = 0		IE-789488-NS-EM1	
		Parts Board (X2)	SW1
(1) Clock that is already mounted on emulation board	32.768 kHz	6-8 shorted	2-3 shorted
(2) Clock that is mounted by user	Other than 32.768 kHz	Oscillator or oscillator circuit assembled by user	
(3) External clock		Oscillator not used	1-2 shorted

The IE-789488-NS-EM1's factory settings are those listed above under "when using clock already mounted on emulation board".

The subsystem clock settings of (1) to (3) are individually described in the following pages.

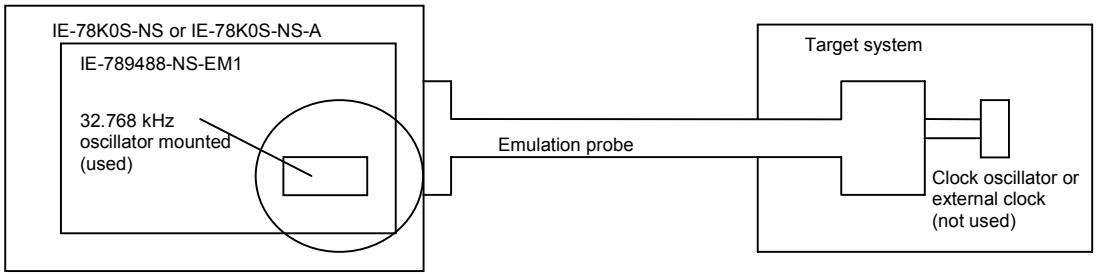
Caution Remove and solder the oscillator on the board or set SW1 to switch between the clock on the board and external clock when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

(1) When using clock already mounted on emulation board

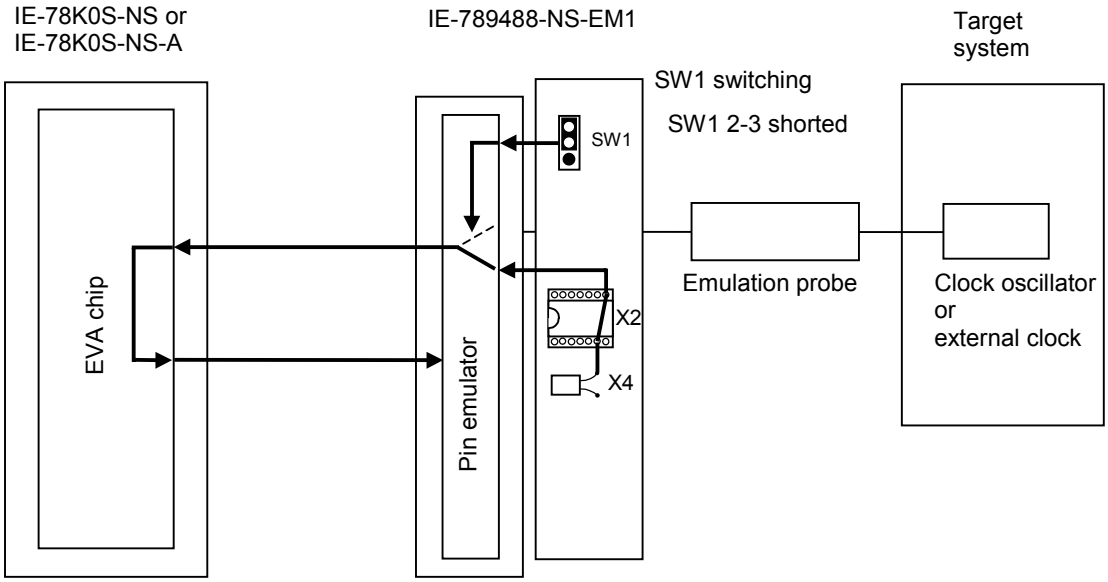
When the IE-789488-NS-EM1 is shipped, a 32.768 kHz crystal oscillator is already mounted on the IE-789488-NS-EM1. SW1 is set to 2-3 shorted, and pins 6 and 8 on the parts board (X2) are shorted.

A setting outline is shown in Figure 3-9.

Figure 3-9. When Using Clock Already Mounted on Emulation Board (Subsystem Clock)



Remark The clock that is supplied by the IE-789488-NS-EM1's oscillator (encircled in the figure) is used.



Remark The flow of the clock is indicated by the bold line.

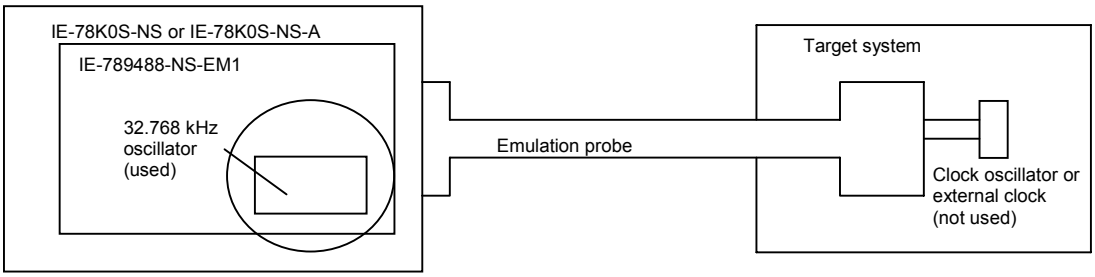
(2) When using clock mounted by user

Remove the crystal oscillator already mounted on the emulation board (X2: 6-8 shorted) and mount the parts board (oscillator) that includes the oscillator or resonator to be used. It is not necessary to change the setting of SW1 2-3 shorted. This is effective when debugging with a clock with a different frequency from the clock already mounted.

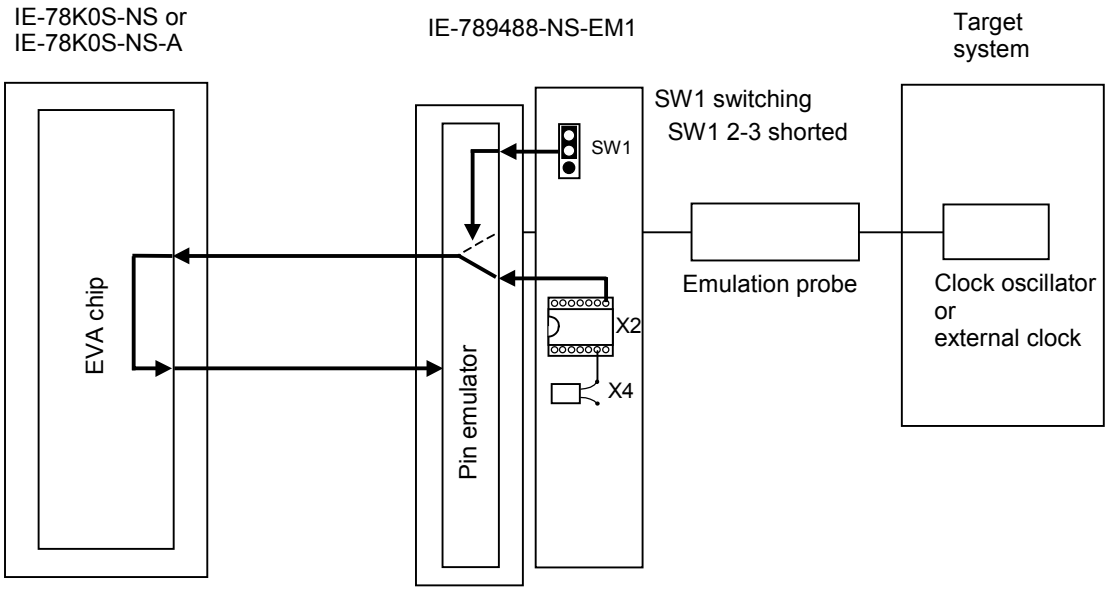
A setting outline is shown in Figure 3-10. The settings of either (a) or (b) that are described in the following pages are required, depending on the type of clock to be used.

Caution When a clock mounted by the user is used, the clock to be used is not multiplied by 4 even if the use of the x4 circuit is specified. Instead, the clock on the board (X3: 131.072 kHz (4.194304/32)) is selected by the IE system.

Figure 3-10. When Using Clock Mounted by User (Subsystem Clock)



Remark The clock that is supplied by the IE-789488-NS-EM1's oscillator (encircled in the figure) is used.



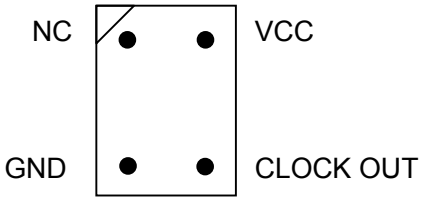
Remark The flow of the clock is indicated by the bold line.

(a) When using a crystal oscillator

♦ Necessary items

• Crystal oscillator (with pin configuration as shown in Figure 3-11)

Figure 3-11. Crystal Oscillator (Subsystem Clock)

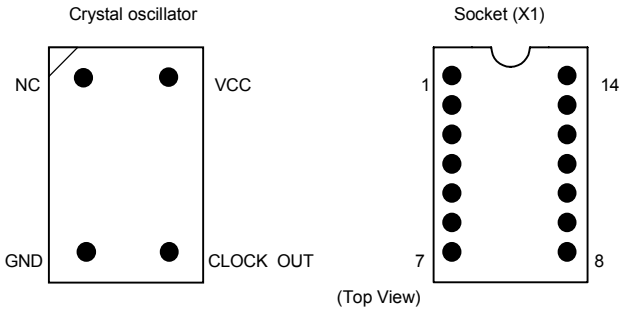


<Procedure>

<1> Prepare the IE-789488-NS-EM1.

<2> Remove the crystal oscillator from the socket (marked X2) on the IE-789488-NS-EM1.

<3> Mount the new crystal oscillator in the socket (X2) from which the oscillator was removed in <2>above. At this time, insert the oscillator into the socket aligning the pins as indicated below.



Crystal Oscillator Pin	Socket Pin No.
NC	1
GND	4
CLOCK OUT	8
VCC	14

<4> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(b) When using a ceramic or crystal resonator

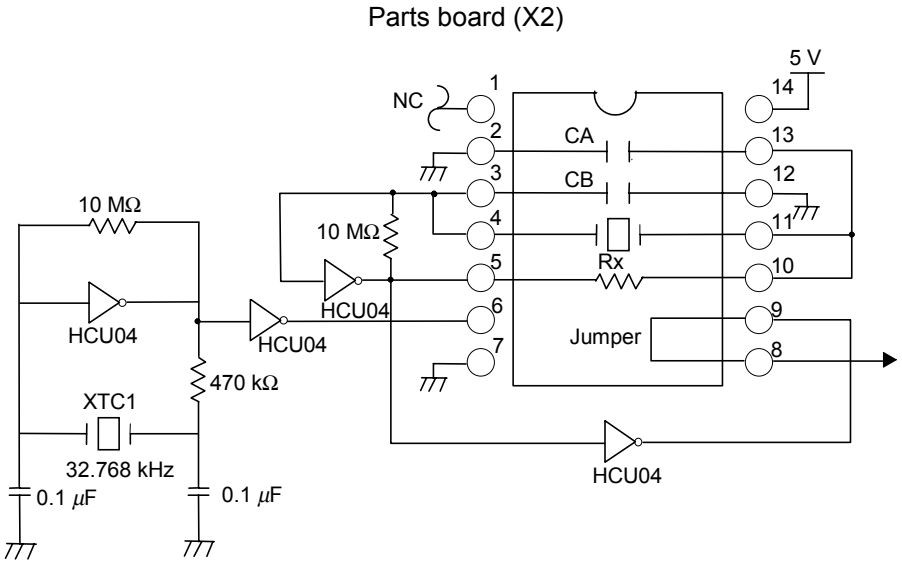
♦ Necessary items

- Parts board
- Ceramic or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Solder kit

<Procedure>

<1> Solder the target ceramic resonator or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board (as shown below).

Figure 3-12. Connections on Parts Board (Subsystem Clock)



Pin No.	Connection
2-13	Capacitor CA
3-12	Capacitor CB
4-11	Resonators
5-10	Resistor Rx
8-9	Shorted

Remark NC: No Connection

<2> Prepare the IE-789488-NS-EM1.

<3> Remove the crystal oscillator that is mounted in the IE-789488-NS-EM1's socket (marked X2).

<4> Connect the parts board (from <1> above) to the socket (X2) from which the crystal oscillator was removed. Check the pin 1 mark to make sure the board is mounted in the correct direction.

<5> Make sure that the parts board mounted in the X2 socket on the emulation board is wired as shown in Figure 3-12 above.

<6> Install the IE-789488-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

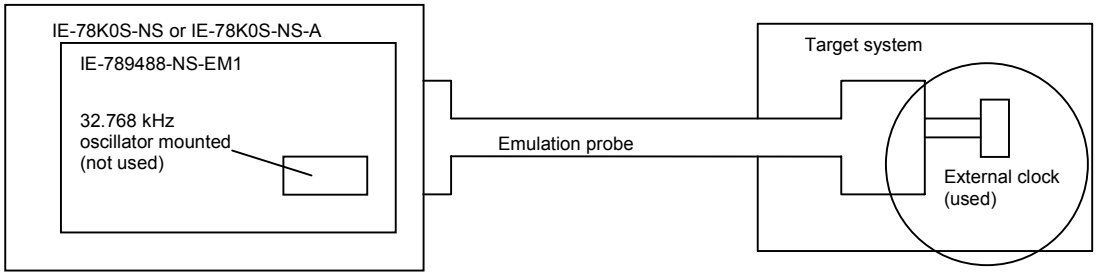
(3) When using an external clock

The external clock pulse signal on the target system is used via an emulation probe. Set SW1 on the IE-789488-NS-EM1 to 1-2 shorted.

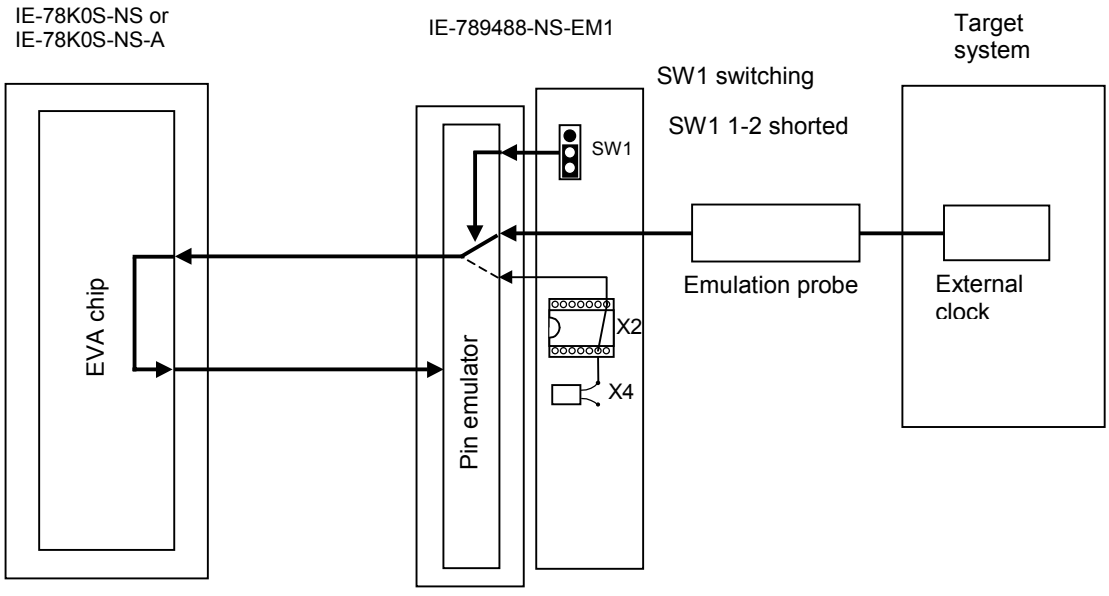
A setting outline is shown in Figure 3-13.

Caution When an external clock is used, the clock to be used is not multiplied by 4 even if the use of the x4 circuit is specified, nor can the clock on the board (X3: 131.072 kHz (4.194304/32)) be selected.

Figure 3-13. When Using External Clock (Subsystem Clock)



Remark The external clock that is supplied by the target system (encircled in the figure) is used.



Remark The flow of the clock is indicated by the bold line.

3.6 Settings of Subsystem Clock x4 Circuit

When using the subsystem clock x4 circuit, the settings vary depending on whether the target to be emulated is a flash memory version or a mask ROM version. Set as described below.

When subsystem clock x4 is selected, the frequency cannot be changed and is fixed to $f_{XTT}/2$ = 131.072 kHz and f_{XT} = 32.768 kHz.

The settings to specify the use of the subsystem clock x4 circuit for a mask ROM version and a flash memory version are shown below.

- For the flash memory version, the setting can be made using bit 0 (SCT) of the SSCK register.
  For details, refer to the user's manual of the target device.
- For the mask ROM version, the setting can be made using a mask option.
  Set the jumper switches (SW3 and SW20).

Table 3-9. Subsystem Clock x4 Circuit Settings

Flash Memory Version	SW3	Bit 0 (SCT) of SSCK Register
Original frequency of subsystem clock 32.768 kHz (changeable)	1-2 (default)	0
Subsystem clock x4 131.072 kHz (fixed)		1
Mask ROM Version	SW3	SW20
Original frequency of subsystem clock 32.768 kHz (changeable)	2-3	2-3 (default)
Subsystem clock x4 131.072 kHz (fixed)		1-2

Cautions 1. Set SW when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

2. The SW20 setting is valid only when the mask ROM version is selected (SW3 2-3 shorted).

3. Use SW20 with the default setting (2-3 shorted) when the flash memory version is selected (SW3 1-2 shorted). This can be changed using bit 0 (SCT) of the SSCK register. For details, refer to the user's manual of the target device.

4. The setting to use the subsystem clock x4 circuit is disabled when using the external clock.

3.7 Setting of Mask Option

3.7.1 Mask option of port 5

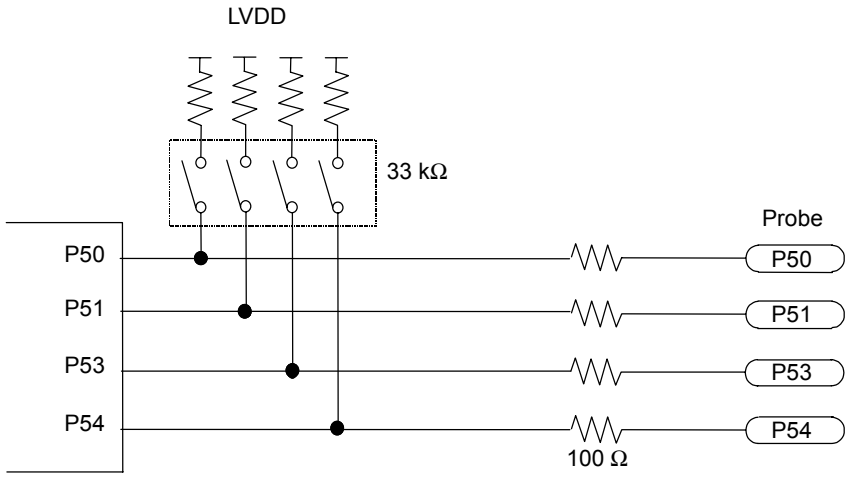
In the IE-789488-NS-EM1, a pull-up resistor of approx. 30 kΩ can be connected to the P50 to P53 pins via a mask option using a DIP switch (SW2).

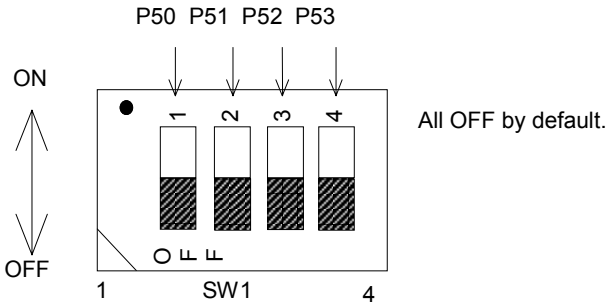
Table 3-10. SW2 Settings

	SW2			
	1	2	3	4
Connected to:	P50	P51	P52	P53

The pins are pulled up to the target voltage (LVDD) when the DIP switch is turned on, and disconnected when the DIP switch is turned off.

Figure 3-14. Mask Option Setting of Port 5





All OFF by default.

3.7.2 Mask option for pin functions

- Port/segment pin switching

  In the IE-789488-NS-EM1, ports and segments can be switched using SW.

  The SW settings are shown in Table 3-11.

Table 3-11. Port/Segment Switching Setting

Port/Segment	Location	Setting
P87	SW8	1-2
S27		1-3, 2-4 (default)
P86	SW9	1-2
S26		1-3, 2-4 (default)
P85	SW10	1-2
S25		1-3, 2-4 (default)
P84	SW11	1-2
S24		1-3, 2-4 (default)
P83	SW12	1-2
S23		1-3, 2-4 (default)
P82	SW13	1-2
S22		1-3, 2-4 (default)
P81	SW14	1-2
S21		1-3, 2-4 (default)
P80	SW15	1-2
S20		1-3, 2-4 (default)
P73	SW19	1-2
S19		1-3, 2-4 (default)
P72	SW18	1-2
S18		1-3, 2-4 (default)
P71	SW17	1-2
S17		1-3, 2-4 (default)
P70	SW16	1-2
S16		1-3, 2-4 (default)

Cautions 1. Segments are selected by default (1-3, 2-4 shorted).

2. Set SW when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

3. When ports are selected, set SW to 3-4 open (if set to 3-4 shorted, the waveforms of the other LCD pins are distorted).

4. In the flash memory version, set SW in addition to setting the port function registers (PF7 and PF8).

3.7.3 Mask option for subsystem clock x4 circuit

The settings to specify the use of the subsystem clock x4 circuit for a mask ROM version are shown below.

The mask option settings are shown in Table 3-12.

Table 3-12. Subsystem Clock x4 Circuit Mask Option Setting

Function	Location	Setting
Mask ROM version selection	SW3	2-3
Subsystem clock x4 (SCTON = 1)	SW20	1-2
Original frequency of subsystem clock (SCTON = 0)		2-3 (default)

Caution Set SW when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

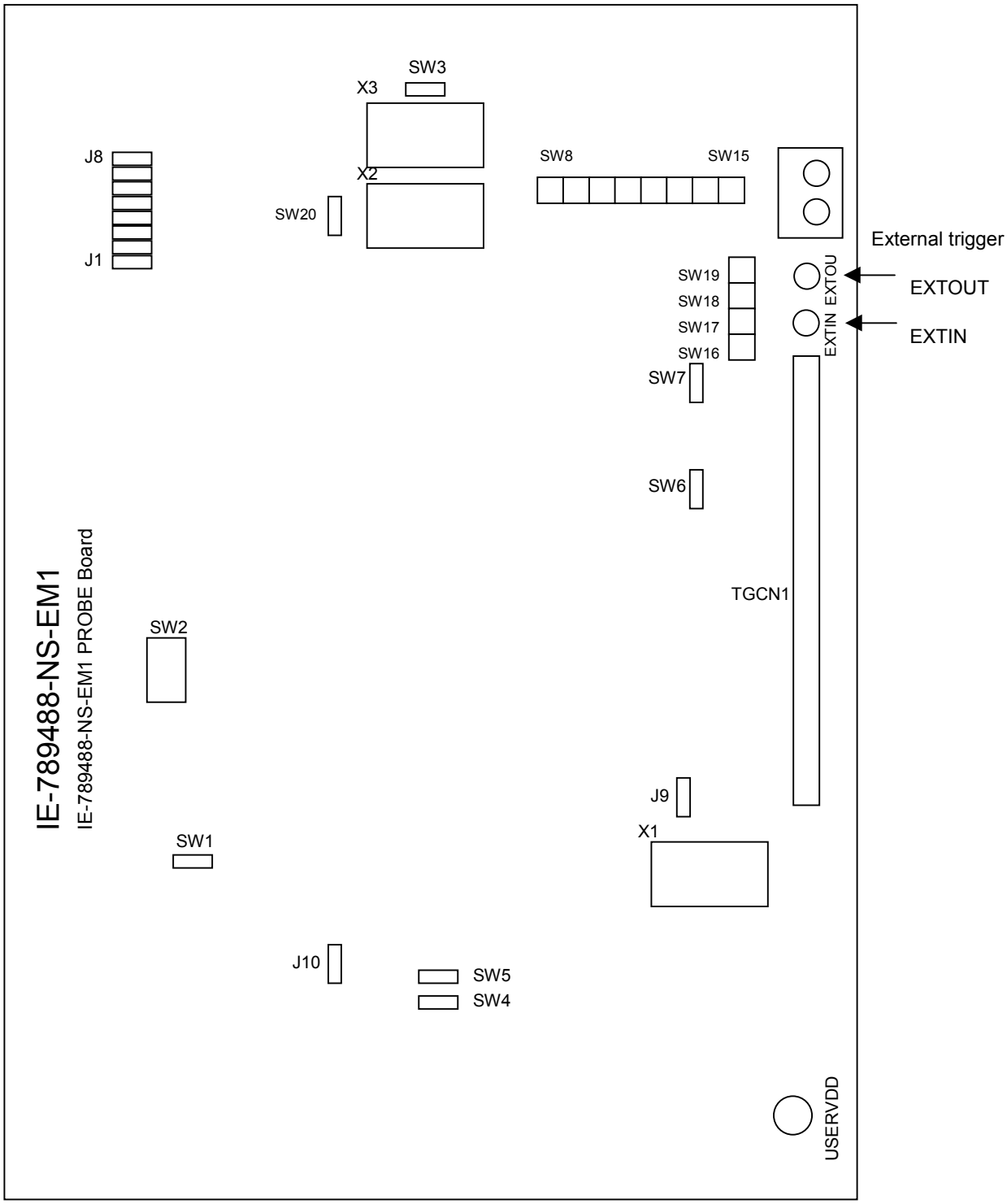
3.8 External Trigger

To set an external trigger, connect it to the IE-789488-NS-EM1's check pin, EXTIN pin, and EXTOUT pin as shown below. The input pin position is shown in Figure 3-15.

See the IE-78K0S-NS or IE-78K0S-NS-A User's Manual for descriptions of pin characteristics.

See the ID78K0S-NS User's Manual for descriptions of usage.

Figure 3-15. External Trigger Input Position



CHAPTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes differences in electrical characteristics between the target device and the target interface circuit.

The target interface circuit of the IE system consists of an EVA chip, FPGA, pin emulator, TTL, CMOS-IC, and other emulation circuits. Differences in electrical characteristics between the target device and the target interface circuit occur due to the existence of a protection circuit.

The differences with the target device are classified into the following (1) to (4) and explained in the following pages.

(1) Signals input/output to/from the pin emulator (target voltage operation)
(2) Signals input from the target system via a gate
(3) Signals related to LCD
(4) Other signals

(1) Signals directly input/output to/from the pin emulator (target voltage operation)

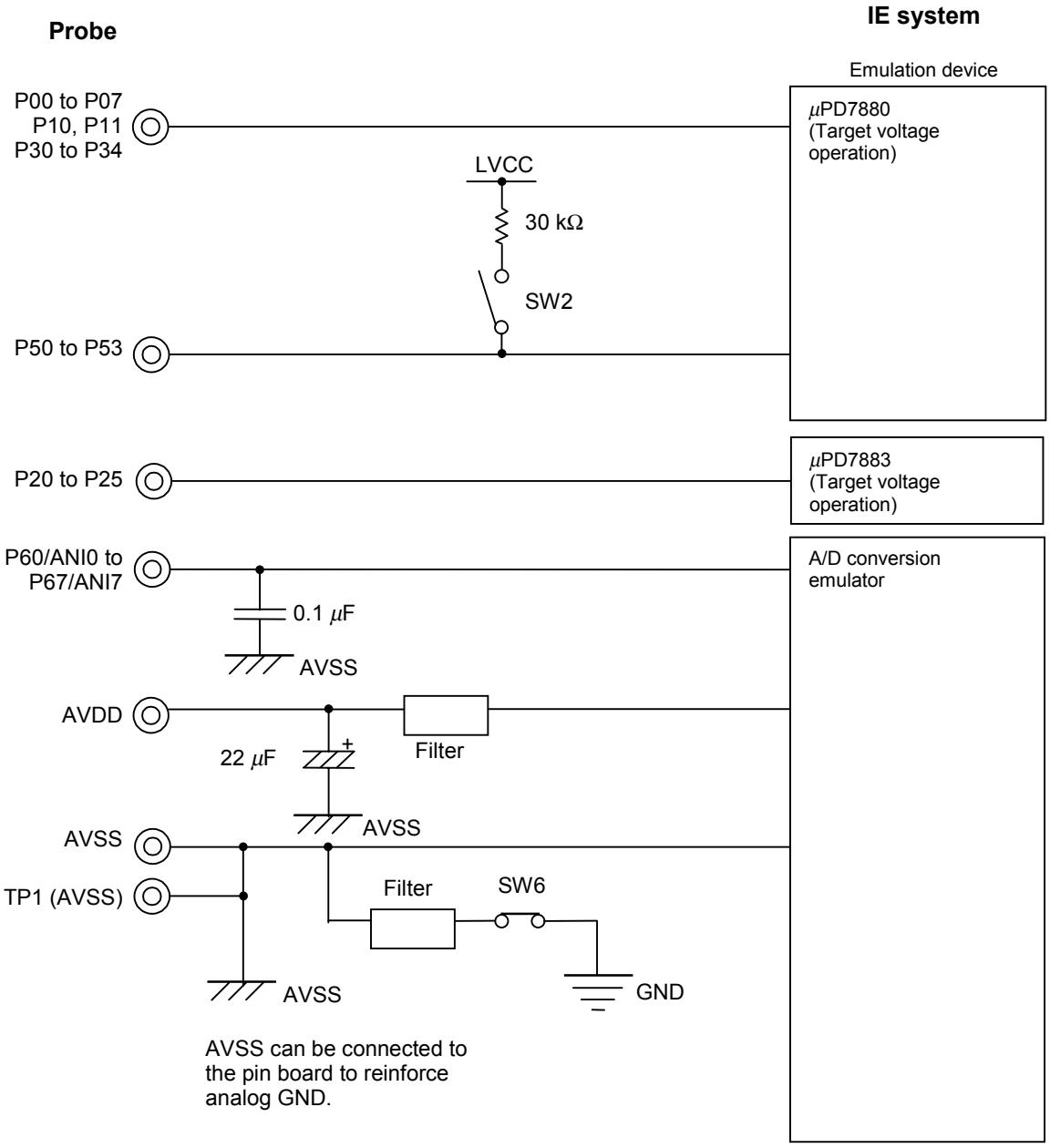
Refer to Figure 4-1 Equivalent Circuit of Emulation Circuit (1).

- Signals related to port 0
- Signals related to port 1
- Signals related to port 3
- Signals related to port 5
- Signals related to port 2
- Signals related to port 6/ANI

  P60/ANI0 to P67/ANI7 can be used to select the μPD789477 or 789488 Subseries via a jumper setting.
- AVDD pin
- AVSS pin

  The AVSS pin from the target system can be connected to the pin board to reinforce GND. The digital and analog ground can be isolated by a switch.

Figure 4-1. Equivalent Circuit of Emulation Circuit (1)



(2) Signals input from the target system via a gate

Refer to Figure 4-2 Equivalent Circuit of Emulation Circuit (2).

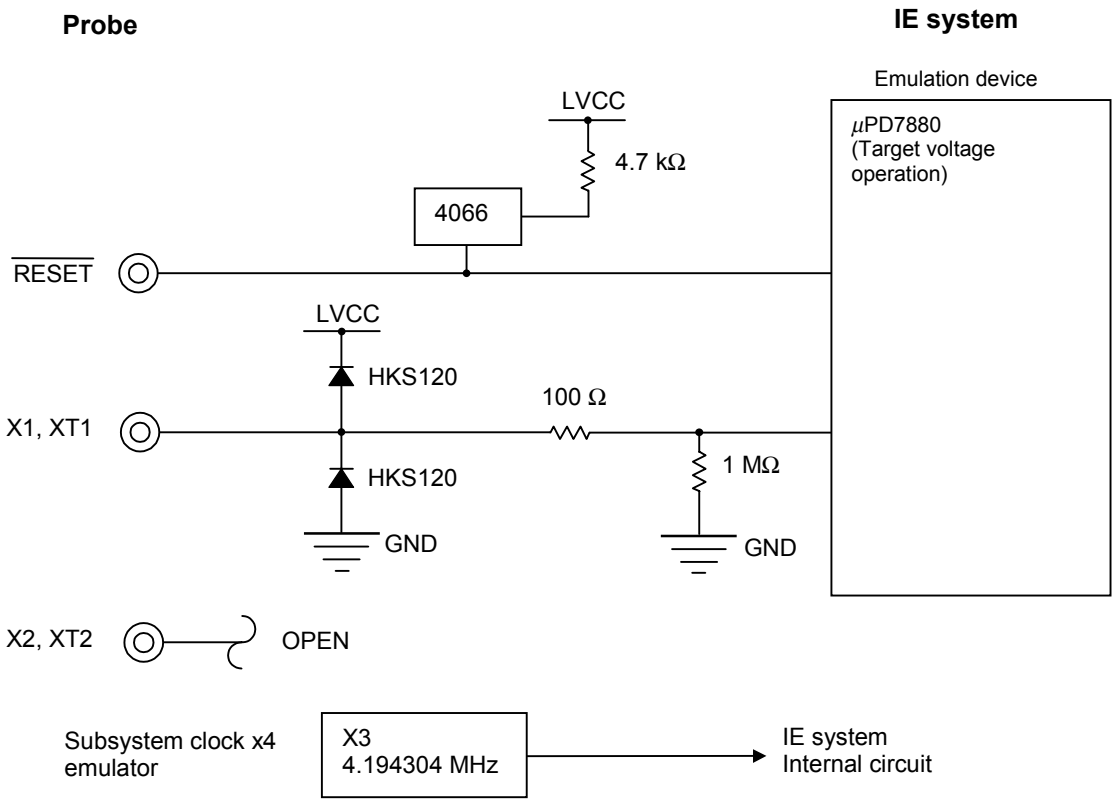
Since the following signals are input via a gate, their timing shows a delay compared to that of the μPD789477 and 789488 Subseries.

- Signals related to RESET
- Signals related to clock input

The XT1 pin is not connected to the x4 circuit.

The IE-789488-NS-EM1 does not use the X2 and XT2 pins.

Figure 4-2. Equivalent Circuit of Emulation Circuit (2)



(3) Signals related to LCD

Refer to Figure 4-3 Equivalent Circuit of Emulation Circuit (3).

- Signals related to port 7/S16 to S19

  Port/segment can be switched via setting S16 to S19.
- Signals related to port 8/S20 to S27

  Port/segment can be switched via setting S8 to S15.
- Signals related to LCD

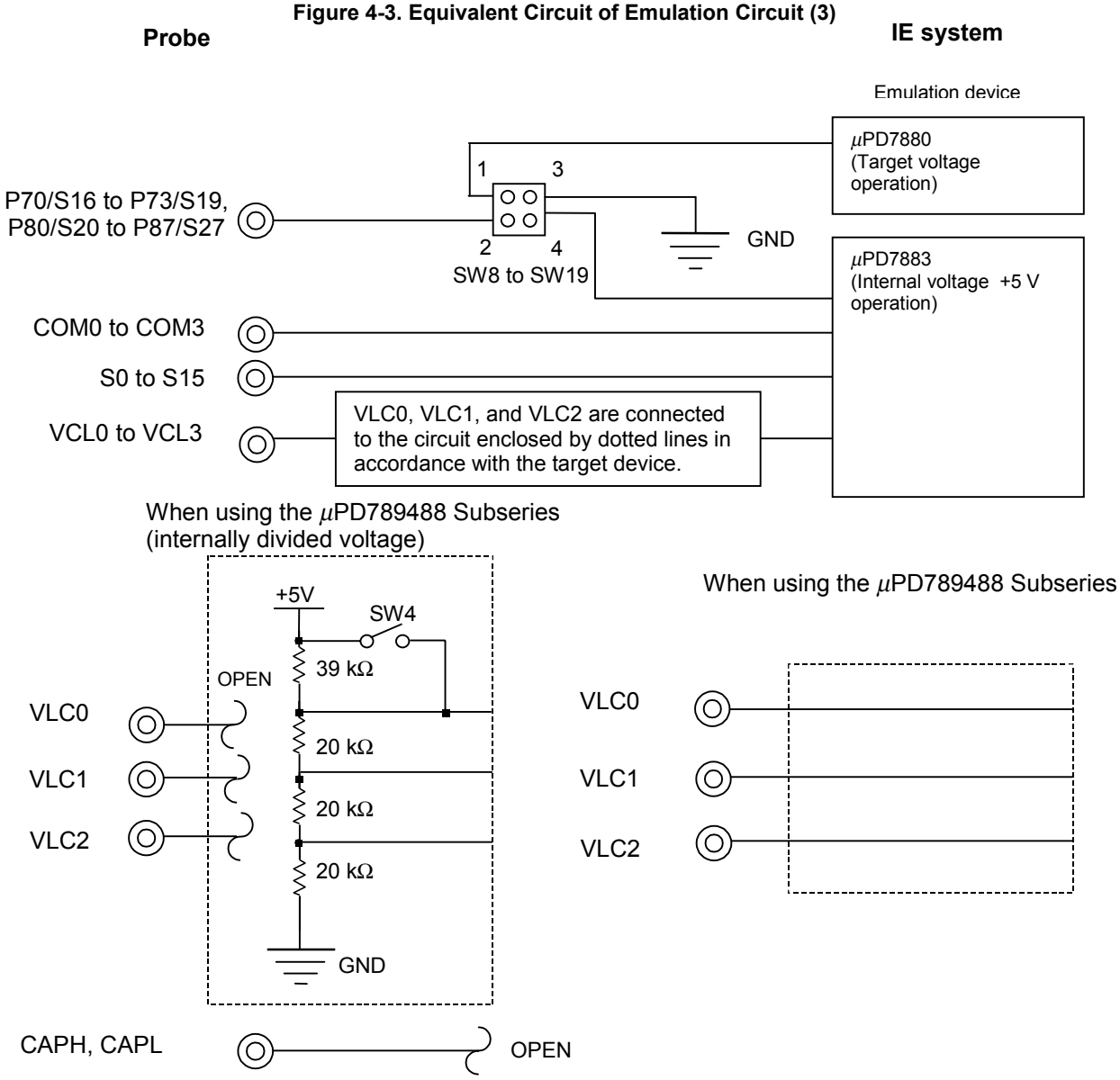
  The target subseries can be switched by VLC0 to VLC2 by setting J9.

  Panel voltage of the μPD789488 Subseries can be set by setting SW4
- CAPH, CAPL signal (μPD789488 Subseries only)

  The target subseries can be switched by VLC0 to VLC2 by setting J9.

  The IE-789488-NS-EM1 does not use these signals.

Figure 4-3. Equivalent Circuit of Emulation Circuit (3)



(4) Other signals

Refer to Figure 4-4 Equivalent Circuit of Emulation Circuit (4).

- VDD pin

When the target system is connected, the target interface power (LVCC) is supplied from the VDD pin.

When the target system is connected, the emulator operates with the internal supply voltage (5 V).

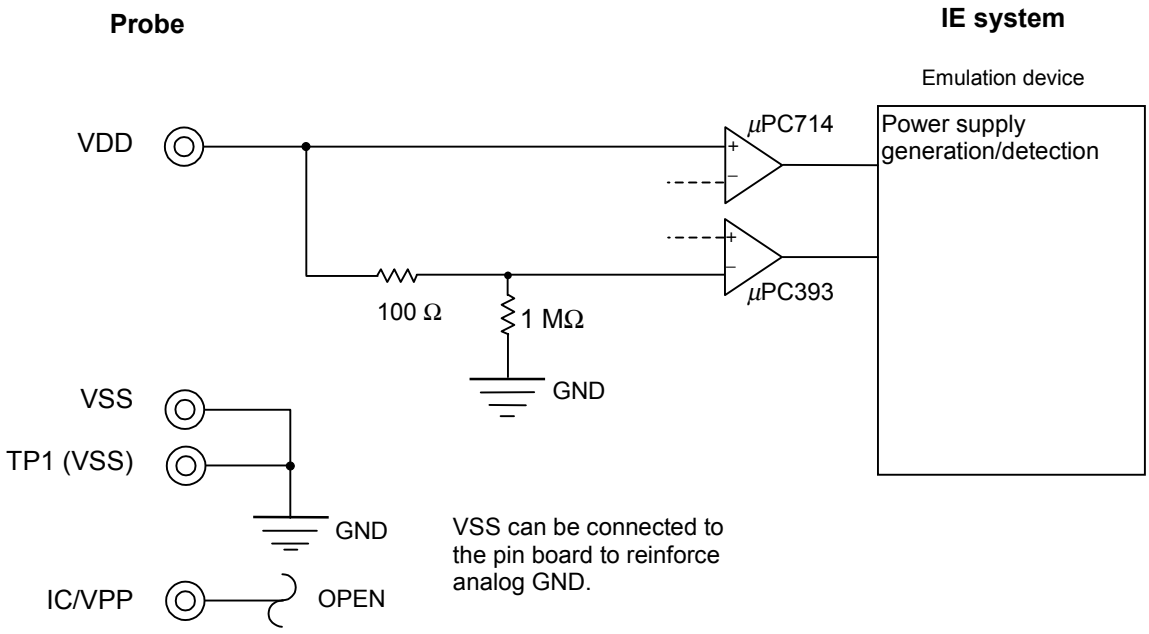
- VSS pin

The V_{SS} pin is connected to GND inside the IE-789488-NS-EM1.

- IC/VPP pin

The IE-789488-NS-EM1 does not use the IC/VPP pin.

Figure 4-4. Equivalent Circuit of Emulation Circuit (4)



CHAPTER 5 CAUTIONS

This chapter describes differences between the target device and the IE system specifications.

The emulation circuit of the IE system consists of an EVA chip, FPGA, pin emulator, TTL, CMOS-IC, and other circuits. Therefore, there are differences between the target device and the IE system specifications.

- Emulation specification when the x4 subsystem clock is selected (1)

  When the x4 subsystem clock is selected, $f_{XTT}/2$ is fixed to 131.072 kHz and f_{XT} is fixed to 32.768 kHz, and these values cannot be changed. Therefore, “using the clock mounted by user” or “using the external clock” cannot be selected.

- Emulation specification when the x4 subsystem clock is selected (2)

  The x4 subsystem clock cannot be stopped by HALT. As a result, the IE-789488-NS-EM1 starts operation one subsystem clock earlier after HALT is released.

- Emulation specification for the port/segment switching mask option

  The port and segment cannot be switched even if the port function registers (PF7 and PF8) are set so.

  In addition to the port function register settings, set SW8 to SW19 in the IE-789488-NS-EM1. For details of the SW settings, refer to **3.7.2 Mask option for pin functions (1) Port/segment pin switching**.

- LCD function specification when emulating the μPD78948x (1)

  It is possible to access bit 6 (VAON0) of LCD display mode register 0 (LCDM0), but the access is not valid. The voltage boost operation is enabled by setting the 9488 mode (J9: 2-3). For details of the jumper setting, refer to **3.3.1 Jumper setting for selecting subseries**.

- LCD function specification when emulating the μPD78948x (2)

  It is possible to access bit 0 (GAIN) of LCD voltage boost control register 0 (LCDVA0), but the access is not valid. The voltage selected by the SW4 setting (LCD panel voltage setting) is always used as the panel voltage. For details of the SW setting, refer to **3.3.2 LCD emulation setting for μPD789488 Subseries**.

APPENDIX A EMULATION PROBE PIN CORRESPONDENCE TABLE

Table A-1. Pin Correspondence of NP-80GC, NP-80GC-TQ, NP-H80GC-TQ, NP-80GK, NP-H80GK-TQ

Emulation Probe Pin No.	TGCN1 Pin No.	Emulation Probe Pin No.	TGCN1 Pin No.
1	114	41	8
2	113	42	7
3	108	43	14
4	107	44	13
5	104	45	18
6	103	46	17
7	100	47	22
8	99	48	21
9	94	49	28
10	93	50	27
11	30	51	92
12	29	52	91
13	24	53	98
14	23	54	97
15	20	55	102
16	19	56	101
17	16	57	106
18	15	58	105
19	10	59	112
20	90	60	111
21	37	61	83
22	43	62	77
23	44	63	78
24	47	64	73
25	48	65	74
26	51	66	69
27	52	67	70
28	57	68	63
29	58	69	64
30	59	70	61
31	60	71	62
32	55	72	65
33	56	73	66
34	49	74	71
35	50	75	72
36	45	76	75
37	46	77	76
38	41	78	79
39	42	79	80
40	35	80	85

Remark NP-80GC, NP-80GC-TQ, NP-H80GC-TQ, NP-80GK, and NP-H80GK-TQ are products of Naito Densei Machida Mfg. Co., Ltd.

APPENDIX B CAUTIONS ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the emulation probe, conversion connector, and conversion socket. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.

Table B-1. Distance from ICE to Conversion Socket

Emulation Probe	Conversion Socket	Distance from ICE to Conversion Socket
NP-80GC	EV-9200GC-80	170 mm
NP-80GC-TQ	TGC-080SBP	170 mm
NP-H80GC-TQ		370 mm
NP-80GK	TGK-080SDP	170 mm
NP-H80GK-TQ		370 mm

Figure B-1. Distance from ICE to Conversion Socket

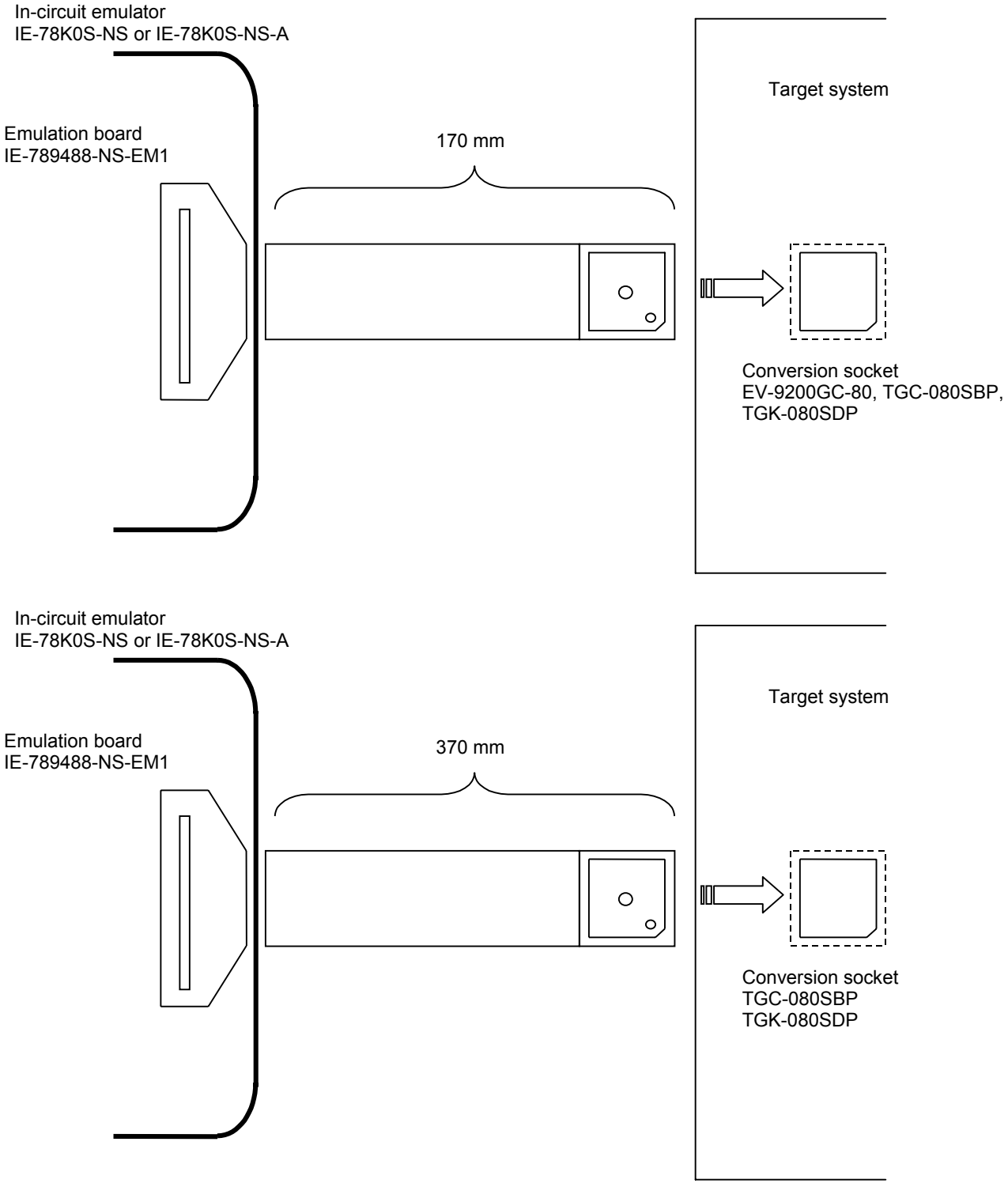


Figure B-2. Conditions for Target System Connection (1)

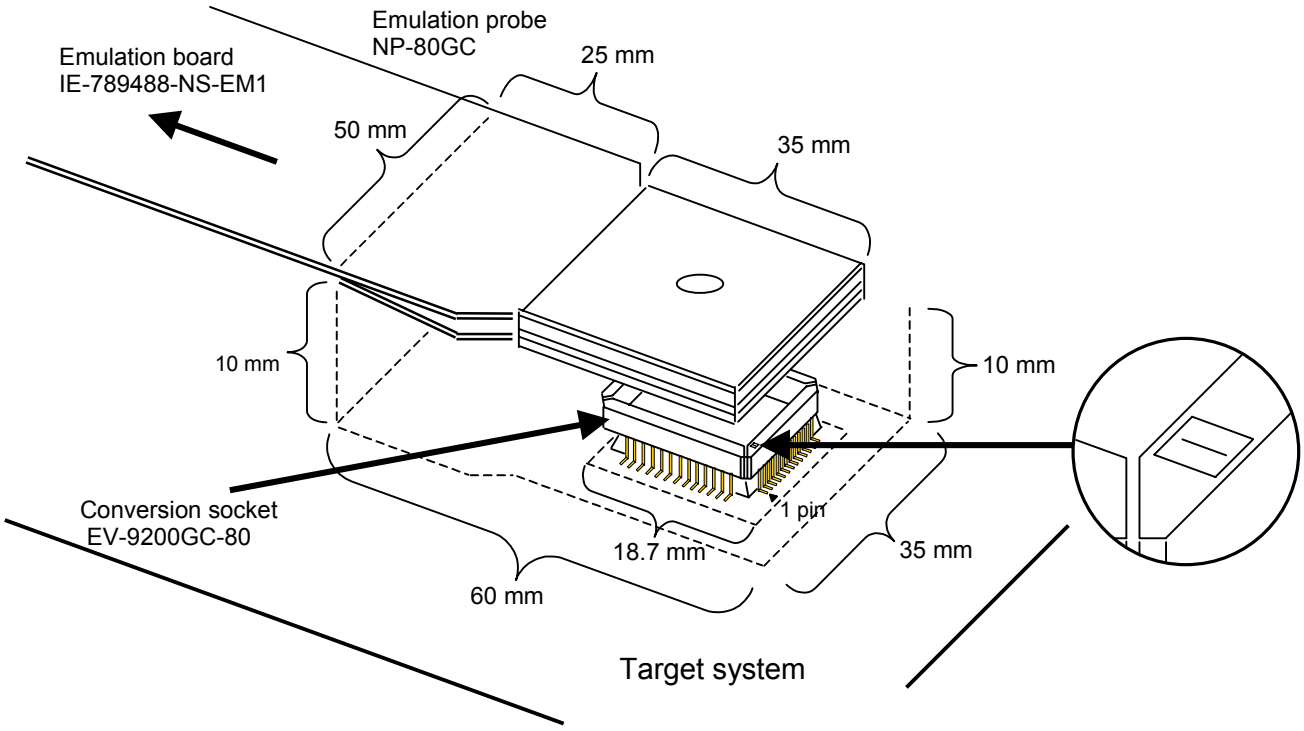


Figure B-3. Conditions for Target System Connection (2)

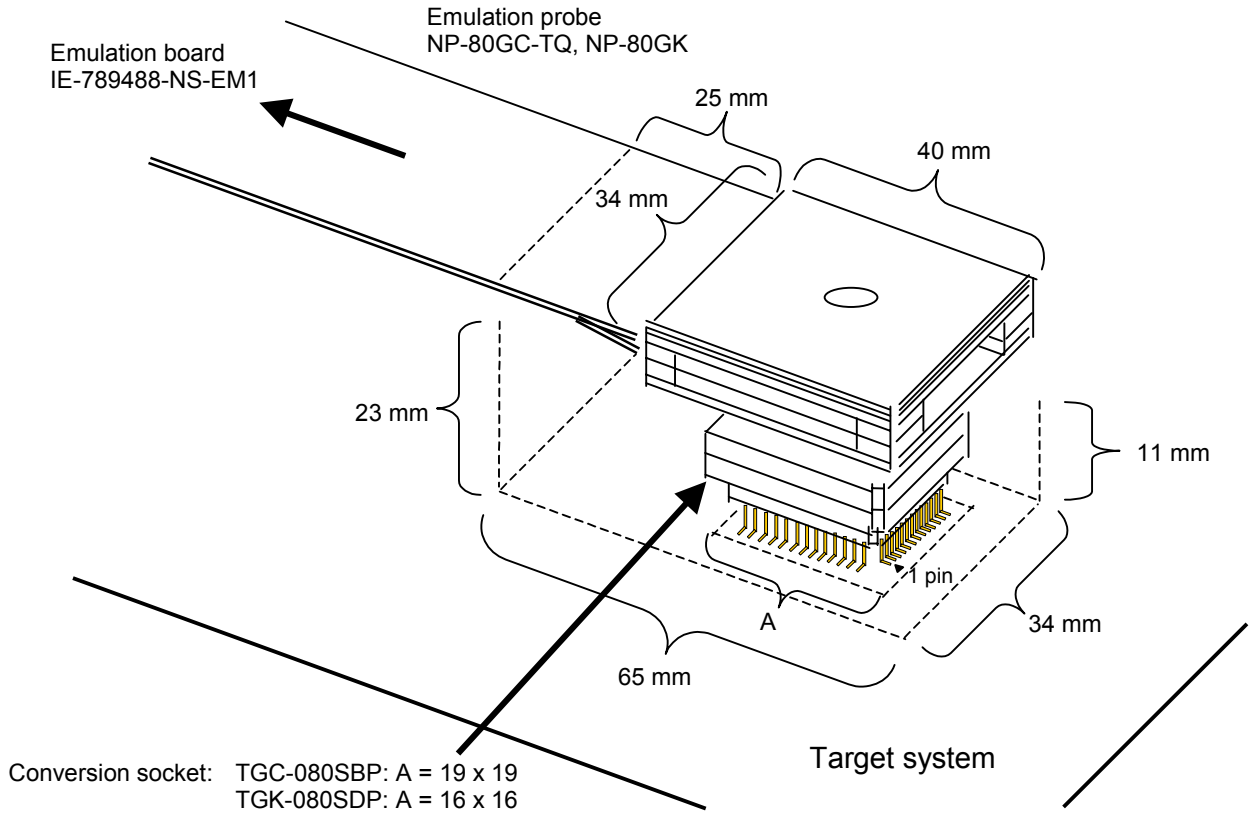
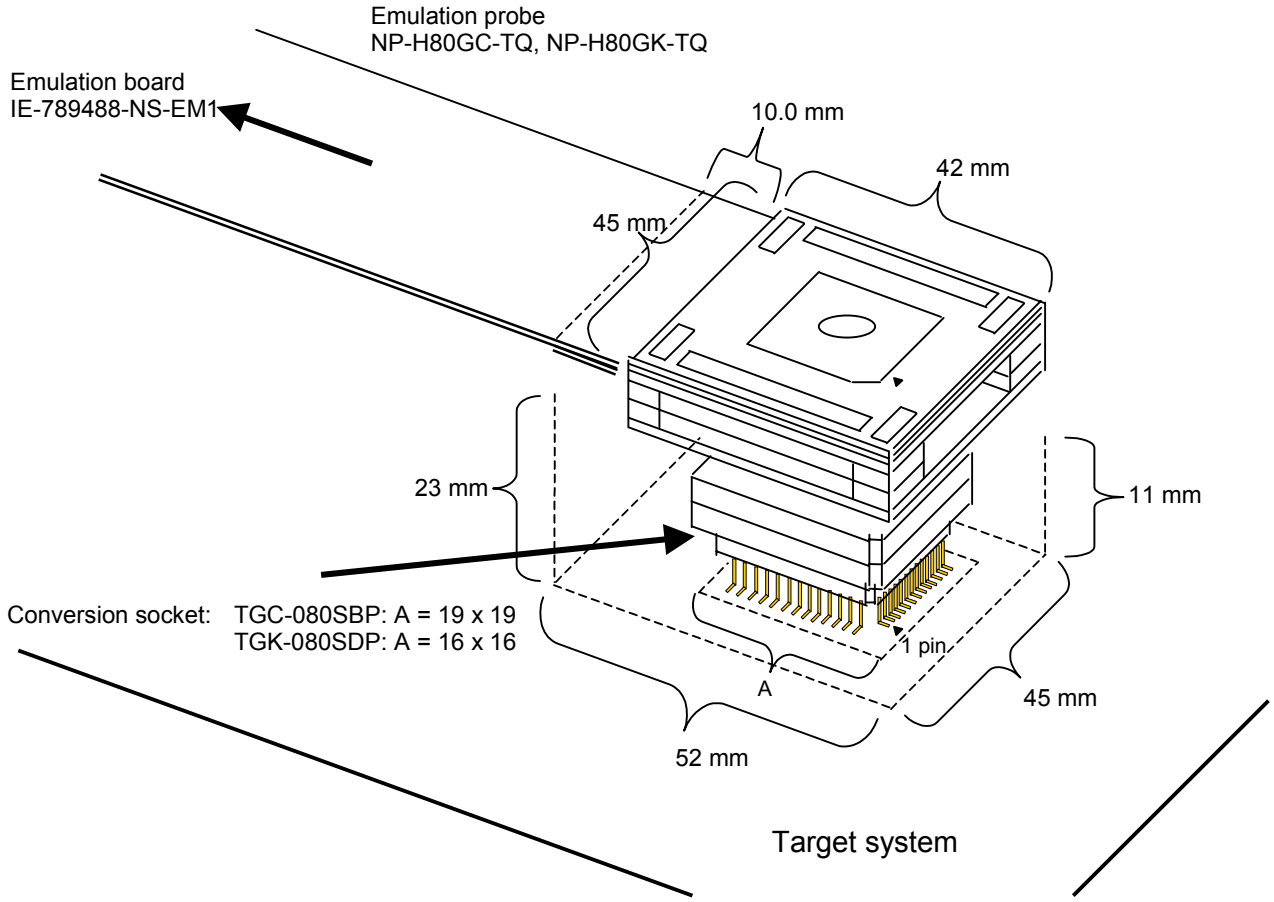


Figure B-4. Conditions for Target System Connection (3)



Remark NP-80GC, NP-80GC-TQ, NP-H80GC-TQ, NP-80GK, and NP-H80GK-TQ are products of Naito Densei Machida Mfg. Co., Ltd.

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