CUSTOMER NOTIFICATION

SUD-DT-03-0254-2-E

October 1, 2003

Yoshiro Harada, Senior System Integrator Microcomputer Group 2nd Solutions Division Solutions Operations Unit NEC Electronics Corporation

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IE-789468-NS-EM1

Preliminary User's Manual

2nd edition, October 2003

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Revision History

The control codes and revised points are listed below.

| Control Code Note | Document No. | Description |
|-------------------|--------------------|--|
| A | SUD-T-4865-1-E | Newly created |
| | (April 7, 2000) | |
| В | SUD-T-4865-2-E | Addition of description on IE-78K0S-NS-A (main board), |
| | (July 17, 2001) | addition of APPENDIX B CAUTIONS ON TARGET SYSTEM |
| | | DESIGN, correction of erroneous description |
| С | SUD-TT-0094-1-E | Addition of description on the emulation CPU setting, |
| | (March 8, 2002) | correction of erroneous description |
| С | SUD-DT-02-0060-1-E | Modification of the IE-789468-NS-EM1 board |
| | (December 5, 2002) | |
| С | SUD-DT-03-0254-1-E | Integration of manuals for new board and old board |
| С | SUD-DT-03-0254-2-E | Correction of erroneous description |
| | (This document) | |

Note The "control code" is the second digit from the left in the 10-digit serial number (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

INTRODUCTION

- Product Overview The IE-789468-NS-EM1 is designed to be used with the IE-78K0S-NS or IE-78K0S-NS-A to debug the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.
 - μPD789327 Subseries: μPD78F9327, 789322, 789324, 789326, 789327
 - μPD789467 Subseries: μPD78F9468, 789462, 789464, 789466, 789467

 Target Readers
 This manual is intended for engineers who will use the IE-789468-NS-EM1 with the IE-78K0S-NS or IE-78K0S-NS-A to perform system debugging.

 Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

• When using the IE-789468-NS-EM1, refer to not only this manual (supplied with the IE-789468-NS-EM1) but also the manual that is supplied with the IE-78K0S-NS or IE-78K0S-NS-A.

This manual is organized as follows.

| IE-78K0S-NS | IE-78K0S-NS-A | IE-789468-NS-EM1 |
|--|--|---|
| User's Manual | User's Manual | User's Manual |
| Basic specifications | Basic specifications | General |
| System configuration | System configuration | Part names |
| External interface | External interface | Installation |
| functions | functions | Differences between |
| | | target devices and target |
| | | interface circuits |
| | | Cautions |

• This manual includes the user's manuals for both the new and old boards. Since the board configuration and settings differ, confirm which board is used in your system when reading this manual.

<How to confirm the board version>

- Products to which a sub-board (IE-789468-NS-EM1 CN board) is connected: New
- Products in which a socket is mounted in the IC1 position: Old

 Purpose
 This manual's purpose is to explain various debugging functions that can be performed when using the IE-789468-NS-EM1.

Terminology

The meanings of certain terms used in this manual are listed below.

| Term | Meaning |
|------------------|--|
| Emulation device | This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU. |
| Emulation CPU | This is the CPU block in the emulator that is used to execute user-generated programs. |
| Target device | This is the device (the real chip) that is the target of emulation. |
| Target system | This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware. |
| IE system | This refers to the combination of the IE-78K0S-NS or IE-78K0S-NS-A and the IE-789468-NS-EM1. |

Conventions

Data significance:Higher digits on the left and lower digits on the rightNote:Footnote for item marked with Note in the textCaution:Information requiring particular attentionRemark:Supplementary information

CONTENTS

I. USER'S MANUAL FOR NEW BOARD

| CHA | PTER 1 GENERAL | . 11 |
|------|---|------|
| 1.1 | System Configuration | .12 |
| 1.2 | Hardware Configuration | .13 |
| 1.3 | Basic Specifications | .14 |
| 1.4 | Emulation CPU | .14 |
| CHA | PTER 2 PART NAMES | .15 |
| 2.1 | Names of Parts on Board | .16 |
| 2.2 | Initial Settings of Switches and Jumpers | . 17 |
| CHAF | PTER 3 INSTALLATION | . 18 |
| 3.1 | Emulation Settings | . 18 |
| | 3.1.1 Settings of emulation CPU | . 18 |
| | 3.1.2 Settings of Switches | .19 |
| 3.2 | Connection | 20 |
| 3.3 | Settings of Switches and Jumpers on Main Board | 21 |
| 3.4 | Settings of Target Interface Voltage | 22 |
| 3.5 | Clock Settings | 23 |
| | 3.5.1 Outline of clock settings | 23 |
| | 3.5.2 Main system clock settings | 25 |
| | 3.5.3 Subsystem clock settings | .31 |
| 3.6 | Mask Option Settings | 37 |
| | 3.6.1 Mask option when μ PD789327 Subseries is debugged | . 37 |
| | 3.6.2 Mask option when μ PD789327, 789467 Subseries is debugged | . 37 |
| 3.7 | External Trigger | . 38 |
| CHA | PTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND | |
| | TARGET INTERFACE CIRCUITS | .39 |
| CHA | PTER 5 CAUTIONS | .43 |
| APPE | ENDIX A EMULATION PROBE PIN ASSIGNMENT TABLE | .44 |
| APPE | ENDIX B CAUTIONS ON TARGET SYSTEM DESIGN | .45 |

II. USER'S MANUAL FOR OLD BOARD

| CHA | PTER 1 GENERAL | |
|------|---|----|
| 1.1 | System Configuration | |
| 1.2 | Hardware Configuration | |
| 1.3 | Basic Specifications | |
| 1.4 | Emulation CPU | |
| CHAI | PTER 2 PART NAMES | |
| 2.1 | Names of Parts on Board | 51 |
| 2.2 | Initial Settings of Switches and Jumpers | |
| CHAI | PTER 3 INSTALLATION | 53 |
| 3.1 | Emulation Settings | |
| | 3.1.1 Settings of emulation CPU | |
| | 3.1.2 Settings of Switches | 54 |
| 3.2 | Connection | |
| 3.3 | Settings of Switches and Jumpers on Main Board | |
| 3.4 | Settings of Target Interface Voltage | 68 |
| 3.5 | Clock Settings | |
| | 3.5.1 Outline of clock settings | |
| | 3.5.2 Main system clock settings | 71 |
| | 3.5.3 Subsystem clock settings | 77 |
| 3.6 | Mask Option Settings | 73 |
| | 3.6.1 Mask option when μ PD789327 Subseries is debugged | 73 |
| | 3.6.2 Mask option when μ PD789327, 789467 Subseries is debugged | 73 |
| 3.7 | External Trigger | 74 |
| CHAI | PTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND | |
| | TARGET INTERFACE CIRCUITS | 75 |
| CHAI | PTER 5 CAUTIONS | 79 |
| APPE | ENDIX A EMULATION PROBE PIN ASSIGNMENT TABLE | |
| APPE | ENDIX B CAUTIONS ON TARGET SYSTEM DESIGN | 81 |

LIST OF FIGURES

I. USER'S MANUAL FOR NEW BOARD

| Figure No. | Title | Page |
|--------------------------|---|------|
| 1-1 System Configura | tion | 12 |
| 1-2 Basic Hardware C | Configuration | 13 |
| 2-1 Names of Parts or | IE-789468-NS-EM1 Board | 16 |
| 3-1 Replacing the Emu | ulation CPU | 18 |
| 3-2 Connection of Em | ulation Probe | 20 |
| 3-3 Connection of TM | 1 and Target System Voltage (When the μ PD789327 Subseries Is Used) | 22 |
| 3-4 External Circuits U | Ised as System Clock Oscillator | 23 |
| 3-5 Outline of System | Clock | 24 |
| 3-6 When Using Clock | Already Mounted on Emulation Board (Main System Clock) | 25 |
| 3-7 When Using Clock | Mounted by User (Main System Clock) | 26 |
| 3-8 Connections on Pa | arts Board (Main System Clock) | 28 |
| 3-9 Crystal Oscillator (| Main System Clock) | 29 |
| 3-10 Correspondence | Between Crystal Oscillator and Socket (Main System Clock) | 29 |
| 3-11 When Inputting a | Clock from Target System (Main System Clock) | 30 |
| 3-12 When Using Cloc | k Already Mounted on Emulation Board (Subsystem Clock) | 31 |
| 3-13 When Using Cloc | k Mounted by User (Subsystem Clock) | 33 |
| 3-14 Connections on F | Parts Board (Subsystem Clock) | 34 |
| 3-15 Crystal Oscillator | (Subsystem Clock) | 35 |
| 3-16 Correspondence | Between Crystal Oscillator and Socket (Subsystem Clock) | 35 |
| 3-17 When Inputting a | Clock from Target System (Subsystem Clock) | 36 |
| 3-18 External Trigger I | nput Position | |
| 4-1 Equivalent Circuit | of Emulation Circuit (1) | 40 |
| 4-2 Equivalent Circuit | of Emulation Circuit (2) | 41 |
| 4-3 Equivalent Circuit | of Emulation Circuit (3) | 42 |
| B-1 Conditions for Targ | et System Connection | 45 |

II. USER'S MANUAL FOR OLD BOARD

| Figure No. | Title | Page |
|----------------------------|---|--------|
| 1-1 System Configuration | on | 47 |
| 1-2 Basic Hardware Co | nfiguration | |
| 2-1 Names of Parts on I | E-789468-NS-EM1 Board | 51 |
| 3-1 Replacing the Emula | ation CPU | 53 |
| 3-2 Connection of Emula | ation Probe | |
| 3-3 Connection of TM1 a | and Target System Voltage (When the μ PD789327 Subseries Is U | sed)58 |
| 3-4 External Circuits Use | ed as System Clock Oscillator | |
| 3-5 Outline of System C | lock | 60 |
| 3-6 When Using Clock A | Already Mounted on Emulation Board (Main System Clock) | 61 |
| 3-7 When Using Clock N | Nounted by User (Main System Clock) | |
| 3-8 Connections on Part | ts Board (Main System Clock) | 64 |
| 3-9 Crystal Oscillator (M | lain System Clock) | 65 |
| 3-10 Correspondence B | etween Crystal Oscillator and Socket (Main System Clock) | 65 |
| 3-11 When Inputting a P | ulse from Target System (Main System Clock) | |
| 3-12 When Using Clock | Already Mounted on Emulation Board (Subsystem Clock) | 67 |
| 3-13 When Using Clock | Mounted by User (Subsystem Clock) | |
| 3-14 Connections on Pa | rts Board (Subsystem Clock) | 70 |
| 3-15 Crystal Oscillator (S | Subsystem Clock) | 71 |
| 3-16 Correspondence B | etween Crystal Oscillator and Socket (Subsystem Clock) | 71 |
| 3-17 When Inputting a P | Pulse from Target System (Subsystem Clock) | 72 |
| 3-18 External Trigger Inp | put Position | 74 |
| 4-1 Equivalent Circuit of | Emulation Circuit (1) | 76 |
| 4-2 Equivalent Circuit of | Emulation Circuit (2) | 77 |
| 4-3 Equivalent Circuit of | Emulation Circuit (3) | 78 |
| B-1 Conditions for Target | t System Connection | 81 |

LIST OF TABLES

I. USER'S MANUAL FOR NEW BOARD

| Tab | e No. | Title | Page |
|-----|--|---------------|------|
| | | | |
| 1-1 | Basic Specifications | | |
| 1-2 | Factory Setting of Emulation CPU | | |
| 2-1 | Initial Settings of Switches and Jumpers | | 17 |
| 3-1 | Setting of Switches and Jumpers on IE-7 | 789468-NS-EM1 | |
| 3-2 | Setting of Switches and Jumpers on IE-7 | 78K0S-NS | |
| 3-3 | Setting of Switches and Jumpers on IE-7 | 78K0S-NS-A | |
| 3-4 | Target Interface Voltage Settings | | |
| 3-5 | Main System Clock Settings | | |
| 3-6 | Subsystem Clock Settings | | |
| 3-7 | Selection of Use of POC Circuit | | |
| A-1 | Pin Assignment of NP-H52GB-TQ | | |

II. USER'S MANUAL FOR OLD BOARD

| Tab | e No. | Title | Page |
|-----|--|---------------|------|
| | | | |
| 1-1 | Basic Specifications | | 49 |
| 1-2 | Factory Setting of Emulation CPU | | 49 |
| | | | |
| 2-1 | Initial Settings of Switches and Jumpers | | 52 |
| | | | |
| 3-1 | Setting of Switches and Jumpers on IE-7 | 789468-NS-EM1 | 55 |
| 3-2 | Setting of Switches and Jumpers on IE-7 | 78K0S-NS | 57 |
| 3-3 | Setting of Switches and Jumpers on IE-7 | 78K0S-NS-A | 57 |
| 3-4 | Target Interface Voltage Settings | | 58 |
| 3-5 | Main System Clock Settings | | 61 |
| 3-6 | Subsystem Clock Settings | | 67 |
| 3-7 | Selection of Use of POC Circuit | | |
| | | | |
| A-1 | Pin Assignment of NP-H52GB-TQ | | 80 |

I. USER'S MANUAL FOR NEW BOARD

See this manual when using the new board (to which the IE-789468-NS-EM1 CN board is connected).

CHAPTER 1 GENERAL

The IE-789468-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

This chapter describes the IE-789468-NS-EM1 system configuration and basic specifications.

- Target devices
 - µPD789327 Subseries
 - μPD789467 Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-789468-NS-EM1 system configuration.



Figure 1-1. System Configuration

- Notes 1. The device files are as follows. μ SXXXDF789328: μ PD789327 Subseries μ SXXXXDF789468: μ PD789467 Subseries
 - The emulation probe is as follows. NP-H52GB-TQ: 52-pin plastic LQFP (probe length: 400 mm; GB type) NP-H52GB-TQ is a product of Naito Densei Machida Mfg. Co., Ltd. Contact: Naito Densei Machida Mfg. Co., Ltd. (TEL: 045-475-4191)
 - The conversion socket and conversion adapter are as follows. TBG-052SBP: For 52-pin plastic LQFP (GB type) TBG-052SBP is a product of Tokyo Eletech Corporation. For further information, contact: Daimaru Kogyo, Ltd. Tokyo Electronics Department (TEL +81-3-3820-7112) Osaka Electronics Department (TEL +81-6-6244-6672)
 - 4. Not used in the IE-789468-NS-EM1.

1.2 Hardware Configuration

Figure 1-2 shows the IE-789468-NS-EM1's position in the basic hardware configuration.



Figure 1-2. Basic Hardware Configuration

1.3 Basic Specifications

The IE-789468-NS-EM1's basic specifications are listed in Table 1-1.

| Parameter | Description | |
|--------------------------|---|--|
| Target device | μPD789327, 789467 Subseries | |
| System clock | Main system clock: 1.000 to 5.000 MHz | |
| | Subsystem clock: 32.768 kHz | |
| Main clock supply | Internal: Mounted on the emulation board (5 MHz) or mounted by user on the parts board | |
| | External: Pulse input from the target system via an emulation probe | |
| Subclock supply | Internal: Mounted on the emulation board (32.768 kHz) or mounted by user on the parts board | |
| | External: Pulse input from the target system via an emulation probe | |
| Target interface voltage | V _{DD} = 1.8 V to 5.5 V (Same as the target device) | |
| | When target system not connected: Operates @ 5 V internal voltage | |

1.4 Emulation CPU

The device (I/O EVA chip) for the emulation CPU varies depending on the subseries as shown in Table 1-2.

The target can be switched by connecting the IE-789468-NS-EM1 CN board, which is included with the IE-789468-NS-EM1. The factory setting is CN101-CN102.

Refer to 3.1.1 Setting of emulation CPU for details of the settings.

Table 1-2. Factory Setting of Emulation CPU

| Target Subseries | Emulation CPU | Factory Setting |
|---------------------|-------------------|-----------------------------|
| | (I/O EVA Chip) | (IE-789468-NS-EM1 CN Board) |
| µPD789327 Subseries | μPD78F9328GK | Connected to CN101-CN102. |
| µPD789467 Subseries | μ PD78F9468GK | CN102-CN103 is left open. |

CHAPTER 2 PART NAMES

This chapter introduces the parts of the IE-789468-NS-EM1 main unit.

The packing box contains the emulation board (IE-789468-NS-EM1), package details, user's manual, and guarantee card.

If there are any missing or damaged items, please contact an NEC Electronics sales representative.

Fill out and return the guarantee card that comes with the main unit.

2.1 Names of Parts on Board

Figure 2-1 shows the names of the parts on the probe board.



Figure 2-1. Names of Parts on IE-789468-NS-EM1 Board

2.2 Initial Settings of Switches and Jumpers

Table 2-1 shows the factory settings of jumpers and switches on the IE-789468-NS-EM1.

Refer to 3.1 Emulation Settings and 3.6 Mask Option Settings for the SW1 setting.

Use SW2 to SW4 with the factory settings.

Refer to 3.5 Clock Settings for the JP1 setting.

| | SW1 | SW2 | SW3 |
|---------|--------|------|------|
| Factory | POC ON | USER | USER |
| setting | | | |

Table 2-1. Initial Settings of Switches and Jumpers

| | SW4-1 | SW4-2 | JP1 |
|---------|-------------|-------------|-----|
| Factory | OFF (fixed) | OFF (fixed) | 2-3 |

Caution R44 is not used.

CHAPTER 3 INSTALLATION

This chapter describes methods for connecting the IE-789468-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A and emulation probe. Mode setting methods are also described.

Caution Connecting or removing parts to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched off.

3.1 Emulation Settings

3.1.1 Setting of emulation CPU

The emulation CPU of the IE-789468-NS-EM1 varies depending on the subseries.

The I/O EVA chip μ PD78F9328GK for debugging the μ PD789327 Subseries is set at shipment. When using the factory-set mode settings, there is no need to make any hardware settings.

When debugging the μ PD789467 Subseries, remove the CN board mounted in CN101-CN102 and mount it in CN102-CN103. The I/O EVA chip μ PD78F9468GK for debugging the μ PD789467 Subseries is then set.



Figure 3-1. Replacing the Emulation CPU

Caution Align the pin 1 position of the connector when mounting the CN board.

Replace the emulation CPU after turning off the power of the IE-78K0S-NS or IE-78K0S-NS-A; otherwise the IE system will be damaged.

3.1.2 Setting of Switches

The switch settings of the IE-789468-NS-EM1 vary depending on the subseries as shown in Table 3-1.

| Table 3-1. | Setting of Switches and Jumpers on IE-789468-NS-EM1 |
|------------|---|
|------------|---|

 μ PD78932x Suberies

| | SW1 | SW2 | SW3 | SW4-1 | SW4-2 | JP1 |
|---------|-------------------------|--------------|--------------|-------------|-------------|------------|
| Setting | POC ON or POC OFF | USER (fixed) | USER (fixed) | OFF (fixed) | OFF (fixed) | 2-3 or 1-2 |

µPD78946x Suberies

| | SW1 | SW2 | SW3 | SW4-1 | SW4-2 | JP1 |
|---------|-------------------------|-------------|-------------|-------------|-------------|------------|
| Setting | POC ON or POC OFF | ICE or USER | ICE or USER | OFF (fixed) | OFF (fixed) | 2-3 or 1-2 |

SW1: Selects use of the POC circuit

POC ON: POC circuit used

POC OFF: POC circuit not used

SW2: Sets the capacitor connected to the V_{LC0} to V_{LC2} pins

ICE: The capacitor on the emulation board is used

USER: The capacitor on the target system is used

SW3: Sets the capacitor connected between the CAPL and CAPH pins

ICE: The capacitor on the emulation board is used

USER: The capacitor on the target system is used

SW4-1, SW4-2: Fixed to OFF

JP1: Sets the subsystem clock

2-3: The clock on the emulation board is used

1-2: The pulse input from the target system is used

Cautions 1. Set the switch after turning off the power of the IE-78K0S-NS or IE-78K0S-NS-A.

2. R44 is not used.

3.2 Connection

A connection diagram of the emulation probe and the main board is shown in Figure 3-2.





(1) Connection with IE-78K0S-NS-A or IE-78K0S-NS-A main unit

See the IE-78K0S-NS User's Manual (U13549E) or IE-78K0S-NS-A User's Manual (U15207E) for a description of how to connect the IE-789468-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A.

(2) Connection with emulation probe

See the IE-78K0S-NS-A User's Manual (U15207E) or IE-78K0S-NS-A User's Manual (U15207E) for a description of how to connect an emulation probe to the IE-789468-NS-EM1.

Connect the emulation probe to CN1 when debugging the μ PD789327 Subseries.

Connect the emulation probe to CN2 when debugging the μ PD789467 Subseries.

Caution Incorrect connection may damage the IE system. For more details on connection, see the user's manual for each emulation probe.

3.3 Settings of Switches and Jumpers on Main Board

(1) Setting of IE-78K0S-NS

Before using the IE-789468-NS-EM1, set each jumper and switch of the IE-78K0S-NS as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS User's Manual (U13549E).

| | SW1 | SW3 | SW4 | JP1 | JP4 |
|---------|-----|----------|----------|-------------|-------------|
| Setting | OFF | All "ON" | All "ON" | 2-3 shorted | 1-2 shorted |
| Setting | OIT | (fixed) | (fixed) | 2-3 shorted | 1-2 Shorted |

Table 3-2. Setting of Switches and Jumpers on IE-78K0S-NS

(2) Setting of IE-78K0S-NS-A

Before using the IE-789468-NS-EM1, set each jumper and switch of the IE-78K0S-NS-A as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS-A User's Manual (U15207E).

Table 3-3. Setting of Switches and Jumpers on IE-78K0S-NS-A

| | SW1 | JP1 | JP3 |
|---------|-----|-------------|-----------------|
| Setting | OFF | 1-2 shorted | Shorted (fixed) |

3.4 Settings of Target Interface Voltage

The IE system can be emulated at the same supply voltage level as that of the target system.

When the target system is not used, the emulator is designed to automatically operate on the internal voltage (5 V). When debugging is performed at the voltage same level as the target system voltage, connect the voltage that is the same level as the target system voltage to the terminal pin (TM1) of the IE-789468-NS-EM1 (also applicable when debugging at 5 V). The status when the μ PD789327 Subseries is debugged is shown in Figure 3-3. The emulation probe is connected to CN2 when debugging the μ PD789467 Subseries.

Set the target voltage to 1.8 to 5.0 V. See ID78K Series Integrated Debugger User's Manual (U15185E) for details of how to select the supply voltage.

The maximum current that can be consumed by TM1 is 1.8 to 5.0 V: approx.125 mA

| Target Interface Voltage | Integrated Debugger (ID78K0S-NS) | |
|------------------------------------|-------------------------------------|----------|
| | Operation Voltage Selection | |
| When the target system is used | 1.8 to 5.5 V | Target |
| When the target system is not used | 5 V | Internal |

Table 3-4. Target Interface Voltage Settings

Figure 3-3. Connection of TM1 and Target System Voltage (When the µPD789327 Subseries Is Used)



Caution Connect TM1 on the board and the target system supply voltage after turning off the power of the IE-78K0S-NS or IE-78K0S-NS-A.

Remark The V_{DD} pin of the target system is only used to control the LED1 that monitors the connection of the target system power supply in the IE-789468-NS-EM1.

3.5 Clock Settings

3.5.1 Outline of clock settings

The main system clock and subsystem clock to be used during debugging can be selected from (1) to (3) below.

- (1) Clock already mounted on emulation board
- (2) Clock mounted by user
- (3) Clock input from the target system

If the target system includes a clock oscillator, select either "(1) Clock already mounted on emulation board" or "(2) Clock mounted by user". For a clock oscillator, the target device is connected to a resonator and the target device's internal oscillator is used. An example of the external circuit is shown in Figure 3-4 (a). During emulation, the clock oscillator that is mounted on the target system is not used. Instead, the clock that is mounted on the emulation board, which is installed for the IE-78K0S-NS or IE-78K0S-NS-A, is used.

If the target system includes an external clock, select either "(1) Clock already mounted on emulation board", "(2) Clock mounted by user", or "(3) Clock input from the target system". For an external clock, a clock signal is supplied from outside of the target device and the target device's internal oscillator is not used. An example of the external circuit is shown in Figure 3-4 (b).

Caution The IE system will hang up if the main system clock is not supplied correctly. In addition, input a rectangular pulse from the target system. It is not necessary to input clock to X2 and XT2 pins. The program does not operate if a crystal or ceramic resonator is connected directly to X1 (in case of main system clock) or XT1 (in case of subsystem clock).

Figure 3-4. External Circuits Used as System Clock Oscillator

(a) Clock oscillator

(b) External clock



An outline of the system clock is shown in Figure 3-5.

Figure 3-5. Outline of System Clock

(a) Main system clock



(b) Subsystem clock



3.5.2 Main system clock settings

The settings of the IE-789468-NS-EM1's main system clock are shown in Table 3-5.

| Frequency of Main System Cl | ock | IE-789468-NS-EM1 | ID78K0S-NS |
|--|---------|-------------------------|----------------------------|
| | | Socket (X1) | CPU Clock Source Selection |
| (1) Clock already mounted on | 5.0 MHz | Oscillator | Internal |
| emulation board | | | |
| (2) Clock mounted by user Other than | | Oscillator assembled or | |
| 5.0 MHz | | prepared by user | |
| (3) Clock input from the target system | | Oscillator (not used) | External |

Table 3-5. Main System Clock Settings

- Caution When using an external clock, open the Configuration dialog box when starting the integrated debugger (ID78K0S-NS) and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).
- **Remark** The IE-789468-NS-EM1's factory settings are those listed above under "when using clock already mounted on emulation board".

(1) When using clock already mounted on emulation board

When the IE-789468-NS-EM1 is shipped, a 5.0 MHz crystal oscillator is already mounted in the IE-789468-NS-EM1's X1 socket. When using the factory-set mode settings, there is no need to make any hardware settings. When starting the integrated debugger (ID78K0S-NS), open the Configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).





Remark The clock that is supplied by the IE-789468-NS-EM1's oscillator (encircled in the figure) is used.

Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

(2) When using clock mounted by user

The settings of either (a) or (b) described in the following pages are required, depending on the type of clock to be used.

When starting the integrated debugger (ID78K0S-NS), open the Configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).





Remark The clock that is supplied by the IE-789468-NS-EM1's oscillator (encircled in the figure) is used.

Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

(a) When using a ceramic or crystal resonator

- Necessary items
 - Crystal or ceramic resonator
- Resistor Rx
- Parts board

- Capacitor CACapacitor CB
- Solder kit

<Procedure>

- <1> Prepare a parts board.
- <2> Solder the target crystal or ceramic resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board as shown below.





Parts board (X1)

| Connection | |
|------------------------------|--|
| Capacitor CA | |
| Capacitor CB | |
| Crystal or ceramic resonator | |
| Resistor Rx | |
| Shorted | |
| | |

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the parts board.
See the resonator data sheets prepared by the resonator manufacturer for details of the values for resistor Rx, capacitor CA, and capacitor CB.

- <3> Prepare the IE-789468-NS-EM1.
- <4> Remove the crystal oscillator that is mounted in the IE-789468-NS-EM1's socket (X1).
- <5> Make sure that the parts board is wired as shown in Figure 3-8 above.
- <6> Connect the parts board (from <2> above) to the socket (X1) from which the crystal oscillator was removed in <4>. Check the pin 1 mark to make sure the board is mounted in the correct direction.
- <7> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(b) When using a crystal oscillator

- Necessary items
 - Crystal oscillator (with pin configuration as shown in Figure 3-9)



Figure 3-9. Crystal Oscillator (Main System Clock)

<Procedure>

GND

- <1> Prepare the IE-789468-NS-EM1.
- <2> Remove the crystal oscillator from the socket (X1) on the IE-789468-NS-EM1.
- <3> Mount the new crystal oscillator in the socket (X1) from which the crystal oscillator was removed in <2>. At this time, insert the crystal oscillator pin into the socket pin as indicated below.



7

CLOCK OUT

| Crystal Oscillator Pin | Socket Pin No. | |
|------------------------|----------------|--|
| NC | 1 | |
| GND | 7 | |
| CLOCK OUT | 8 | |
| Vcc | 14 | |
| | | |

<4> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

8

(3) Clock input from the target system

There is no need to make any hardware settings.

When starting the integrated debugger (ID78K0S-NS), open the Configuration dialog box and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user clock).





Remark The clock that is supplied by the external clock (encircled in the figure) is used.



Outline Diagram

Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

3.5.3 Subsystem clock settings

The settings of the IE-789468-NS-EM1's subsystem clock are shown in Table 3-6.

| Frequency of Subsystem Clo | ock | IE-789468-NS-EM1 | |
|---|--------------------------|-----------------------------|--------------|
| | | Socket (X2) | Jumper (JP1) |
| (1) Clock that is already mounted on emulation board (XTC1) | 32.768 kHz | 6-8 shorted | 2-3 shorted |
| (2) Clock that is mounted by user | Other than 32.768 kHz | Oscillator prepared by user | |
| (3) Clock input from the target system | | Oscillator not used | 1-2 shorted |

Table 3-6. Subsystem Clock Settings

Caution Set JP1 to switch between the clock on the board and external clock after turning off the power of the IE-78K0S-NS or IE-78K0S-NS-A.

Remark The IE-789468-NS-EM1's factory settings are those listed above under "when using clock already mounted on emulation board".

(1) When using clock already mounted on emulation board

When the IE-789468-NS-EM1 is shipped, a crystal resonator (XTC1) is already mounted on the IE-789468-NS-EM1. When using the factory-set mode settings, there is no need to make any hardware settings. Pins 6 and 8 of the IE-789468-NS-EM1's socket (X2) on the parts board (X2) are shorted. Set the jumper (JP1) to 2-3 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).





Remark The clock that is supplied by the IE-789468-NS-EM1's resonator (encircled in the figure) is used.

Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the socket (X2).

(2) When using clock mounted by user

The settings of either (a) or (b) described in the following pages are required, depending on the type of clock to be used. Set the jumper (JP1) on the IE-789468-NS-EM1 to 2-3 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).





Remark The clock that is supplied by the IE-789468-NS-EM1's oscillator (encircled in the figure) is used.



Outline Diagram

Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

(a) When using a crystal resonator

- Necessary items
- Crystal resonator
- Resistor Rx
- Parts board

- Capacitor CACapacitor CB
- Solder kit

- <Procedure>
- <1> Prepare a parts board.
- <2> Solder the target crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board as shown below.





| Pin No. | Connection |
|---------|-------------------|
| 2-13 | Capacitor CA |
| 3-12 | Capacitor CB |
| 4-11 | Crystal resonator |
| 5-10 | Resistor Rx |
| 8-9 | Shorted |

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the parts board. See the resonator data sheets prepared by the resonator manufacturer for details of the values for resistor Rx, capacitor CA, and capacitor CB.

- <3> Prepare the IE-789468-NS-EM1.
- <4> Remove the jumper that is mounted in the IE-789468-NS-EM1's socket (X2).
- <5> Make sure that the parts board is wired as shown in Figure 3-14 above.
- <6> Connect the parts board (from <2> above) to the socket (X2) from which the jumper was removed in <4>. Check the pin 1 mark to make sure the board is mounted in the correct direction.
- <7> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(b) When using a crystal oscillator

- Necessary items
- Crystal oscillator (with pin configuration as shown in Figure 3-15)





<Procedure>

- <1> Prepare the IE-789468-NS-EM1.
- <2> Remove the jumper from the socket (X2) on the IE-789468-NS-EM1.
- <3> Mount the crystal oscillator in the socket (X2) from which the jumper was removed in <2>. At this time, insert the crystal oscillator pin into the socket pin as indicated below.

Figure 3-16. Correspondence Between Crystal Oscillator and Socket (Subsystem Clock)



| Crystal Oscillator Pin | Socket Pin No. |
|------------------------|----------------|
| NC | 1 |
| GND | 7 |
| CLOCK OUT | 8 |
| Vcc | 14 |

<4> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(3) When using a clock input from the target system

The external clock pulse signal on the target system is used via an emulation probe. Set JP1 on the IE-789468-NS-EM1 to 1-2 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).





Remark The external clock that is supplied by the target system (encircled in the figure) is used.

Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.
3.6 Mask Option Settings

3.6.1 Mask option when μ PD789327 Subseries is debugged

In the IE-789468-NS-EM1, the oscillation stabilization time, which is set by a mask option in the μ PD789327 Subseries, cannot be selected. The oscillation stabilization wait time is the same as that of the flash memory version, μ PD78F9327.

• Oscillation stabilization time: 2¹⁵/fx (fixed)

3.6.2 Mask option when μ PD789327, 789467 Subseries is debugged

In the IE-789468-NS-EM1, whether to use the POC circuit, which is set by a mask option in the μ PD789327, 789467 Subseries, can be selected. The switch settings are shown in Table 3-7.

Table 3-7. Selection of Use of POC Circuit

| POC Circuit | SW1 |
|-------------------------|-------------------------------|
| POC circuit is used | POC ON side (default setting) |
| POC circuit is not used | POC OFF side |

Caution Set the switch after turning off the power of the IE-78K0S-NS or IE-78K0S-NS-A.

3.7 External Trigger

To set an external trigger, connect it to the IE-789468-NS-EM1's check pin, EXTOUT pin and EXTIN pin. The input pin position is shown in Figure 3-18.

See the IE-78K0S-NS User's Manual (U13549E) or IE-78K0S-NS-A User's Manual (U15207E) for descriptions of pin characteristics.

See the ID78K Series Integrated Debugger Ver.2.30 or Later Operation User's Manual (Windows[™] Based) (U15185E) for descriptions of usage.

(1) EXTOUT

A low-level pulse is output from the IE-789468-NS-EM1's EXTOUT pin for 1.3 μ s upon the occurrence of a break event.

Caution Because this is an open-drain output, a pull-up resistor should be connected on the target system.

(1) EXTIN

An event signal can be input from the IE-789468-NS-EM1's EXTIN pin. Input a high-level pulse signal for 2 CPU operating clocks or longer.



Figure 3-18. External Trigger Input Position

CHAPTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes differences in electrical characteristics between the target device and the target interface circuit.

The target interface circuit of the IE system consists of an emulation CPU, TTL, CMOS-IC, and other emulation circuits. Differences in electrical characteristics between the target device and the target interface circuit occur due to the existence of a protection circuit.

- (1) Signals directly input/output to/from the EVA chip and peripheral EVA chip
- (2) Signals input from the target system via a gate
- (3) Other signals

The circuits of the IE-789468-NS-EM1 for the signals in (1) to (3) above are shown below.

(1) Signals directly input/output to/from the EVA chip and peripheral EVA chip

Refer to Figure 4-1 Equivalent Circuit of Emulation Circuit (1).

The following signals operate in the same manner as those in the μ PD789327, 789467 Subseries.

- Signals related to port 0
- Signals related to port 1
- Signals related to port 4
- Signals related to port 6
- Signals related to port 8 (S17 to S22)
- S0 to S16
- COM0 to COM3

A pull-up resistor of 1 M Ω is directly inserted in the following signal.

• Signals related to port 2 (µPD789327 Subseries only)

Figure 4-1. Equivalent Circuit of Emulation Circuit (1)

Probe side(Target system)

♦ IE system



(2) Signals input from the target system via a gate

Since the following signals are input via a gate, their timing shows a delay compared to that of the µPD789327,

789467 Subseries. Refer to Figure 4-2 Equivalent Circuit of Emulation Circuit (2).

- Signals related to RESET
- Signals related to clock input

The IE-789468-NS-EM1 does not use the X2 and XT2 pins.

- CAPH, CAPL (µPD789467 Subseries only)
- VLc0 to VLc2 (VLc1 and VLc2 are available in the μPD789467 Subseries only)



Figure 4-2. Equivalent Circuit of Emulation Circuit (2)

(3) Other signals

Refer to Figure 4-3 Equivalent Circuit of Emulation Circuit (3).

• VDD pin

When the target system is not connected, the power supply of the emulation CPU operates with the internal supply voltage (5 V). When the target system is connected, it operates with the power (LVcc) supplied from the low-voltage supply pin (TM1).

The V_{DD} pin of the target system is only used to control the LED1 (USER VDD) that monitors the connection of the target system power supply in the IE-789468-NS-EM1.

Vss pin

The Vss pin is connected to GND inside the IE-789468-NS-EM1.

• IC/VPP pin

The IE-789468-NS-EM1 does not use the IC/VPP pin.



Figure 4-3. Equivalent Circuit of Emulation Circuit (3)

CHAPTER 5 CAUTIONS

This chapter describes differences between the target device and the IE system specifications.

The emulation circuit of the IE system consists of an EVA chip, TTL, CMOS-IC, and other circuits. Therefore, there are differences between the target device and the IE system specifications.

• Read value of port 2 when the target system is not connected

Port 2 of the μ PD789327 Subseries is directly connected to a 1 M Ω pull-up resistor. When the port value is read in input mode when the target system is not connected, the value read from port 2 is 07h.

• Oscillation stabilization wait time cannot be changed

The oscillation stabilization wait time of the μ PD789327 Subseries (mask ROM version) after STOP mode is released by RESET input or power-on clear is the same as that of the μ PD78F9328 (flash memory version).

• Oscillation stabilization time: 2¹⁵/fx (fixed)

APPENDIX A EMULATION PROBE PIN ASSIGNMENT TABLE

| Emulation Probe Pin No. | CN1 Pin No. | Emulation Probe Pin No. | CN1 Pin No. |
|----------------------------|-------------|----------------------------|-------------|
| 1 | 118 | 31 22 | |
| 2 | 114 | 32 | 28 |
| 3 | 108 | 33 | 92 |
| 4 | 104 | 34 | 91 |
| 5 | 100 | 35 | 98 |
| 6 | 94 | 36 | 102 |
| 7 | 30 | 37 | 106 |
| 8 | 29 | 38 | 112 |
| 9 | 24 | 39 | 116 |
| 10 | 20 | 40 | 87 |
| 11 | 16 | 41 | 83 |
| 12 | 10 | 42 | 77 |
| 13 | 6 | 43 | 73 |
| 14 | 33 | 44 | 69 |
| 15 | 37 | 45 | 63 |
| 16 | 43 | 46 | 61 |
| 17 | 47 | 47 | 65 |
| 18 | 51 | 48 | 71 |
| 19 | 57 | 49 | 75 |
| 20 | 59 | 50 | 79 |
| 21 | 55 | 51 | 85 |
| 22 | 49 | 52 | 89 |
| 23 | 45 | | |
| 24 | 41 | | |
| 25 | 35 | | |
| 26 | 31 | | |
| 27 | 4 | | |
| 28 | 8 | | |
| 29 | 14 | | |
| 30 | 18 | | |

Table A-1. Pin Assignment of NP-H52GB-TQ

Remark NP-H52GB-TQ is a product of Naito Densei Machida Mfg. Co., Ltd.

APPENDIX B CAUTIONS ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the emulation probe, conversion connector, and conversion socket. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.







II. USER'S MANUAL FOR OLD BOARD

See this manual when using the old board.

CHAPTER 1 GENERAL

The IE-789468-NS-EM1 is a development tool for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K0S Series of 8-bit single-chip microcontrollers.

This chapter describes the IE-789468-NS-EM1 system configuration and basic specifications.

- Target device
 - µPD789327 Subseries
 - µPD789467 Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-789468-NS-EM1 system configuration.



Figure 1-1. System Configuration

- Notes 1. The device files are as follows. μ SXXXDF789328: μ PD789327 Subseries μ SXXXXDF789468: μ PD789467 Subseries
 - The emulation probe is as follows. NP-H52GB-TQ: 52-pin plastic LQFP (probe length: 400 mm; GB type) NP-H52GB-TQ is a product of Naito Densei Machida Mfg. Co., Ltd. Contact: Naito Densei Machida Mfg. Co., Ltd. (TEL: 045-475-4191)
 - The conversion socket and conversion adapter are as follows. TBG-052SBP: For 52-pin plastic LQFP (GB type) TBG-052SBP is a product of Tokyo Eletech Corporation. For further information, contact: Daimaru Kogyo, Ltd. Tokyo Electronics Department (TEL +81-3-3820-7112) Osaka Electronics Department (TEL +81-6-6244-6672)
 - 4. Not used in the IE-789468-NS-EM1.

1.2 Hardware Configuration

Figure 1-2 shows the IE-789468-NS-EM1's position in the basic hardware configuration.





1.3 Basic Specifications

The IE-789468-NS-EM1's basic specifications are listed in Table 1-1.

| Parameter | Description | | | |
|--------------------------|---|--|--|--|
| Target device | μPD789327, 789467 Subseries | | | |
| System clock | Main system clock: 1.000 to 5.000 MHz | | | |
| | Subsystem clock: 32.768 kHz | | | |
| Main clock supply | Internal: Mounted on the emulation board (5 MHz) or mounted by user on the parts board | | | |
| | External: Pulse input from the target system via an emulation probe | | | |
| Subclock supply | Internal: Mounted on the emulation board (32.768 kHz) or mounted by user on the parts board | | | |
| | External: Pulse input from the target system via an emulation probe | | | |
| Target interface voltage | V _{DD} = 1.8 V to 5.5 V (Same as the target device) | | | |
| | When target system not connected: Operates @ 5 V internal voltage | | | |

1.4 Emulation CPU

The device (I/O EVA chip) for the emulation CPU varies depending on the subseries as shown in Table 1-2.

Refer to **2.1 Names of Parts on Board** for details of the IC1 position. Refer to **3.1.1 Setting of emulation CPU** for details of the settings. The I/O EVA chip μ PD78F9468GK E1.3 used for debugging the μ PD789467 Subseries is supplied with the IE-789468-NS-EM1.

Table 1-2. Factory Setting of Emulation CPU

| Target Subseries | Emulation CPU | Factory Setting |
|--------------------------|--------------------|--|
| | (I/O EVA Chip) | |
| μ PD789327 Subseries | μPD78F9328GK V1.31 | Mounted in the socket (IC1) on the board |
| µPD789467 Subseries | μPD78F9468GK E1.3 | Included with the IE-789468-NS-EM1 |

CHAPTER 2 PART NAMES

This chapter introduces the parts of the IE-789468-NS-EM1 main unit.

The packing box contains the emulation board (IE-789468-NS-EM1), case (emulation CPU ^{Note 1}), screw driver ^{Note 2}), package details, user's manual, and guarantee card.

If there are any missing or damaged items, please contact an NEC Electronics sales representative.

Fill out and return the guarantee card that comes with the main unit.

Notes 1. The emulation CPU is as follows.

μPD789327 Subseries: I/O EVA chip μPD78F9328GK V1.31 (Mounted in IC1 on the emulation board at shipment) μPD789467 Subseries: I/O EVA chip μPD78F9468GK E1.3 (Included with the IE-789468-NS-EM1at shipment)

2. Screw driver

This is a screw driver used to remove/fix the screws used to fix the socket (IC1) that incorporates the emulation CPU.

2.1 Names of Parts on Board

Figure 2-1 shows the names of the parts on the probe board.





2.2 Initial Settings of Switches and Jumpers

Table 2-1 shows the initial settings of jumpers and switches on the IE-789468-NS-EM1.

Refer to 3.1 Emulation Settings and 3.6 Mask Option Settings for the SW1 setting.

Use SW2 to SW4 with the default settings.

Refer to 3.5 Clock Settings for the JP1 setting.

| | SW1 | SW2 | SW3 |
|-----------------|-------------|-------------|-----|
| Initial setting | POC ON | USR | USR |
| | SW4 to SW1 | SW4 to SW2 | JP1 |
| Initial setting | OFF (fixed) | OFF (fixed) | 2-3 |

Caution R44 is not used.

CHAPTER 3 INSTALLATION

This chapter describes methods for connecting the IE-789468-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A and emulation probe. Mode setting methods are also described.

Caution Connecting or removing parts to or from the target system, or making switch or other setting changes must be carried out after the power supply to both the IE system and the target system has been switched off.

3.1 Emulation Settings

3.1.1 Setting of emulation CPU

The emulation CPU of the IE-789468-NS-EM1 varies depending on the subseries.

The I/O EVA chip μ PD78F9328GK V1.31 for debugging the μ PD789327 Subseries is mounted in the socket (IC1) at shipment. When using the factory-set mode settings, there is no need to make any hardware settings. When debugging the μ PD789467 Subseries, remove the I/O EVA chip μ PD78F9328GK V1.31 for debugging the μ PD789327 Subseries from the socket (IC1) and mount the I/O EVA chip μ PD78F9468GK E1.3 for debugging the μ PD789467 Subseries which is included with the IE-789468-NS-EM1 in the socket (IC1).

Each pin of the I/O EVA chip is fixed within the plastic partition by the NQPACK080SD contact pin and the HQPACK080SD hold pin. Therefore, I/O EVA chip pins placed side by side will never be shorted.



Figure 3-1. Replacing the Emulation CPU

<Procedure>

- (1) Remove the four screws (M2 \times 6 mm) fixing the HQPACK080SD from the HQPACK080SD using the supplied screw driver.
- (2) Remove the mounted I/O EVA chip.
- (3) Mount the I/O EVA chip corresponding to the subseries to be debugged. (Set the I/O EVA chip so that the pin 1 position of the I/O EVA chip and NQPACK080SD match.)
- (4) Set the HQPACK080SD and fix it to the I/O EVA chip and NQPACK080SD using the four screws (M2 × 6 mm). Fix the screws using the supplied screw driver or a screw driver with a torque gauge in the order of opposite diagonals and applying equal pressure to all four corners (be careful not to fix one screw too tightly). The

torque for tightening a screw is 0.55 kg \cdot f \cdot cm (0.054 N \cdot m) MAX. Fixing a screw too tightly may cause bad conduction.

- Cautions 1. Replace the emulation CPU when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off; otherwise the IE system will be damaged.
 - 2. When mounting the emulation CPU, set it so that the pin 1 position of the I/O EVA chip and the socket (IC1) match; otherwise the emulation CPU will be damaged.
 - 3. The emulation CPU does not operate correctly if the I/O EVA chip is mounted with bent leads.
 - 4. Before the I/O EVA chip is mounted on the NQPACK052SB, make sure that there are no abnormalities such as resin burr, bent pins, or crooked pins. When the I/O EVA chip is covered by the HQPACK080SD, make sure that there are no crooked or bent HQPACK080SD hold pins before mounting. If there are bent or crooked pins, straighten the pins by using a flat surface like an edge of a knife.

3.1.2 Setting of Switches

The switch settings of the IE-789468-NS-EM1 vary depending on the subseries as shown in Table 3-1.

| Table 3-1. | Setting of Switches and Jumpers on IE-789468-NS-EM1 |
|------------|---|
|------------|---|

 μ PD78932x Suberies

| | SW1 | SW2 | SW3 | SW4-1 | SW4-2 | JP1 |
|---------|-------------------------|--------------|--------------|-------------|-------------|------------|
| Setting | POC ON or POC OFF | USER (fixed) | USER (fixed) | OFF (fixed) | OFF (fixed) | 2-3 or 1-2 |

µPD78946x Suberies

| | SW1 | SW2 | SW3 | SW4-1 | SW4-2 | JP1 |
|---------|-------------------------|-------------|-------------|-------------|-------------|------------|
| Setting | POC ON or POC OFF | ICE or USER | ICE or USER | OFF (fixed) | OFF (fixed) | 2-3 or 1-2 |

SW1: Selects use of the POC circuit

POC ON: POC circuit used

POC OFF: POC circuit not used

SW2: Sets the capacitor connected to the V_{LC0} to V_{LC2} pins

ICE: The capacitor on the emulation board is used

USER: The capacitor on the target system is used

SW3: Sets the capacitor connected between the CAPL and CAPH pins

ICE: The capacitor on the emulation board is used

USER: The capacitor on the target system is used

SW4-1, SW4-2: Fixed to OFF

JP1: Sets the subsystem clock

2-3: The clock on the emulation board is used

1-2: The pulse input from the target system is used

Cautions 1. Set the switch after turning off the power of the IE-78K0S-NS or IE-78K0S-NS-A.

2. R44 is not used.

3.2 Connection

A connection diagram of the emulation probe and the main board is shown in Figure 3-2.





(1) Connection with IE-78K0S-NS-A or IE-78K0S-NS-A main unit

See the IE-78K0S-NS User's Manual (U13549E) or IE-78K0S-NS-A User's Manual (U15207E) for a description of how to connect the IE-789468-NS-EM1 to the IE-78K0S-NS or IE-78K0S-NS-A.

(2) Connection with emulation probe

See the IE-78K0S-NS-A User's Manual (U15207E) or IE-78K0S-NS-A User's Manual (U15207E) for a description of how to connect an emulation probe to the IE-789468-NS-EM1. Connect the emulation probe to CN1 when debugging the μ PD789327 Subseries. Connect the emulation probe to CN2 when debugging the μ PD789467 Subseries.

Caution Incorrect connection may damage the IE system. For more details on connection, see the user's manual for each emulation probe.

3.3 Settings of Switches and Jumpers on Main Board

(1) Setting of IE-78K0S-NS

Before using the IE-789468-NS-EM1, set each jumper and switch of the IE-78K0S-NS as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS User's Manual (U13549E).

| | SW1 | SW3 | SW4 | JP1 | JP4 |
|---------|-----|----------|----------|-------------|-------------|
| Setting | OFF | All "ON" | All "ON" | 2-3 shorted | 1-2 shorted |
| Setting | OIT | (fixed) | (fixed) | 2-3 shorted | 1-2 Shorted |

Table 3-2. Setting of Switches and Jumpers on IE-78K0S-NS

(2) Setting of IE-78K0S-NS-A

Before using the IE-789468-NS-EM1, set each jumper and switch of the IE-78K0S-NS-A as described below. For the positions of the switches and jumpers, refer to the IE-78K0S-NS-A User's Manual (U15207E).

Table 3-3. Setting of Switches and Jumpers on IE-78K0S-NS-A

| | SW1 | JP1 | JP3 |
|---------|-----|-------------|-----------------|
| Setting | OFF | 1-2 shorted | Shorted (fixed) |

3.4 Settings of Target Interface Voltage

The IE system can be emulated at the same supply voltage level as that of the target system.

When the target system is not used, the emulator is designed to automatically operate on the internal voltage (5 V). When debugging is performed at the voltage same level as the target system voltage, connect the voltage that is the same level as the target system voltage to the terminal pin (TM1) of the IE-789468-NS-EM1 (also applicable when debugging at 5 V). The status when the μ PD789327 Subseries is debugged is shown in Figure 3-3. The emulation probe is connected to CN2 when debugging the μ PD789467 Subseries.

Set the target voltage to 1.8 to 5.0 V. See ID78K Series Integrated Debugger User's Manual (U15185E) for details of how to select the supply voltage.

The maximum current that can be consumed by TM1 is 1.8 to 5.0 V: approx.125 mA

| Target Interface Voltage | | Integrated Debugger (ID78K0S-NS) |
|------------------------------------|--------------|-------------------------------------|
| | | Operation Voltage Selection |
| When the target system is used | 1.8 to 5.5 V | Target |
| When the target system is not used | 5 V | Internal |

Table 3-4. Target Interface Voltage Settings

Figure 3-3. Connection of TM1 and Target System Voltage (When the µPD789327 Subseries Is Used)



Caution Connect TM1 on the board and the target system supply voltage when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

Remark The V_{DD} pin of the target system is only used to control the LED1 that monitors the connection of the target system power supply in the IE-789468-NS-EM1.

3.5 Clock Settings

3.5.1 Outline of clock settings

The main system clock and subsystem clock to be used during debugging can be selected from (1) to (3) below.

- (1) Clock already mounted on emulation board
- (2) Clock mounted by user
- (3) Pulse input from the target system

If the target system includes a clock oscillator, select either "(1) Clock already mounted on emulation board" or "(2) Clock mounted by user". For a clock oscillator, the target device is connected to a resonator and the target device's internal oscillator is used. An example of the external circuit is shown in Figure 3-4 (a). During emulation, the clock oscillator that is mounted on the target system is not used. Instead, the clock that is mounted on the emulation board, which is installed for the IE-78K0S-NS or IE-78K0S-NS-A, is used.

If the target system includes an external clock, select either "(1) Clock already mounted on emulation board", "(2) Clock mounted by user", or "(3) Pulse input from the target system". For an external clock, a clock signal is supplied from outside of the target device and the target device's internal oscillator is not used. An example of the external circuit is shown in Figure 3-4 (b).

Caution The IE system will hang up if the main system clock is not supplied correctly. In addition, input a rectangular pulse from the target system. It is not necessary to input clock to X2 and XT2 pins. The program does not operate if a crystal or ceramic resonator is connected directly to X1 (in case of main system clock) or XT1 (in case of subsystem clock).

Figure 3-4. External Circuits Used as System Clock Oscillator

(a) Clock oscillator

(b) External clock



An outline of the system clock is shown in Figure 3-5.

Figure 3-5. Outline of System Clock

(a) Main system clock



(b) Subsystem clock



3.5.2 Main system clock settings

The settings of the IE-789468-NS-EM1's main system clock are shown in Table 3-5.

| Frequency of Main System Cl | ock | IE-789468-NS-EM1 | ID78K0S-NS |
|--|------------|-------------------------|----------------------------|
| | | Socket (X1) | CPU Clock Source Selection |
| (1) Clock already mounted on | 5.0 MHz | Oscillator | Internal |
| emulation board | | | |
| (2) Clock mounted by user | Other than | Oscillator assembled or | |
| | 5.0 MHz | prepared by user | |
| (3) Pulse input from the target system | | Oscillator (not used) | External |

Table 3-5. Main System Clock Settings

- Caution When using an external clock, open the configuration dialog box when starting the integrated debugger (ID78K0S-NS) and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).
- **Remark** The IE-789468-NS-EM1's factory settings are those listed above under "when using clock already mounted on emulation board".

(1) When using clock already mounted on emulation board

When the IE-789468-NS-EM1 is shipped, a 5.0 MHz crystal oscillator is already mounted in the IE-789468-NS-EM1's X1 socket. When using the factory-set mode settings, there is no need to make any hardware settings. When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).





Remark The clock that is supplied by the IE-789468-NS-EM1's oscillator (encircled in the figure) is used.

Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

(2) When using clock mounted by user

The settings of either (a) or (b) described in the following pages are required, depending on the type of clock to be used.

When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select "Internal" in the area (Clock) for selecting the CPU's clock source (this selects the emulator's internal clock).





Remark The clock that is supplied by the IE-789468-NS-EM1's oscillator (encircled in the figure) is used.

Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

(a) When using a ceramic or crystal resonator

- Necessary items
 - Crystal or ceramic resonator
- Resistor Rx
- Parts board

- Capacitor CACapacitor CB
- Solder kit

<Procedure>

- <1> Prepare a parts board.
- <2> Solder the target crystal or ceramic resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board as shown below.

Figure 3-8. Connections on Parts Board (Main System Clock)



| Connection |
|------------------------------|
| Capacitor CA |
| Capacitor CB |
| Crystal or ceramic resonator |
| Resistor Rx |
| Shorted |
| |

Parts board (X1)

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the parts board.
See the resonator data sheets prepared by the resonator manufacturer for details of the values for resistor Rx, capacitor CA, and capacitor CB.

- <3> Prepare the IE-789468-NS-EM1.
- <4> Remove the crystal oscillator that is mounted in the IE-789468-NS-EM1's socket (X1).
- <5> Make sure that the parts board is wired as shown in Figure 3-8 above.
- <6> Connect the parts board (from <2> above) to the socket (X1) from which the crystal oscillator was removed in <4>. Check the pin 1 mark to make sure the board is mounted in the correct direction.
- <7> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(b) When using a crystal oscillator

- Necessary items
 - Crystal oscillator (with pin configuration as shown in Figure 3-9)



Figure 3-9. Crystal Oscillator (Main System Clock)

- <Procedure>
- <1> Prepare the IE-789468-NS-EM1.
- <2> Remove the crystal oscillator from the socket (X1) on the IE-789468-NS-EM1.
- <3> Mount the new crystal oscillator in the socket (X1) from which the crystal oscillator was removed in <2>. At this time, insert the crystal oscillator pin into the socket pin as indicated below.

Figure 3-10. Correspondence Between Crystal Oscillator and Socket (Main System Clock)



| Crystal Oscillator Pin | Socket Pin No. |
|------------------------|----------------|
| NC | 1 |
| GND | 4 |
| CLOCK OUT | 8 |
| Vcc | 14 |

<4> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(3) When using a pulse input from the target system

There is no need to make any hardware settings.

When starting the integrated debugger (ID78K0S-NS), open the configuration dialog box and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user clock).





Remark The clock that is supplied by the external clock (encircled in the figure) is used.



Outline Diagram

Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

3.5.3 Subsystem clock settings

The settings of the IE-789468-NS-EM1's subsystem clock are shown in Table 3-6.

| Frequency of Subsystem Clo | Frequency of Subsystem Clock | | IE-789468-NS-EM1 | |
|--|------------------------------|------------------------|------------------|--|
| | | Socket (X2) | Jumper (JP1) | |
| (1) Clock that is already mounted on | 32.768 kHz | 6-8 shorted | 2-3 shorted | |
| emulation board (XTC1) | | | | |
| (2) Clock that is mounted by user | Other than | Oscillator prepared by | | |
| | 32.768 kHz | user | | |
| (3) Pulse input from the target system | | Oscillator not used | 1-2 shorted | |

Table 3-6. Subsystem Clock Settings

Caution Set JP1 to switch between the clock on the board and external clock when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

Remark The IE-789468-NS-EM1's factory settings are those listed above under "when using clock already mounted on emulation board".

(1) When using clock already mounted on emulation board

When the IE-789468-NS-EM1 is shipped, a crystal resonator (XTC1) is already mounted on the IE-789468-NS-EM1. When using the factory-set mode settings, there is no need to make any hardware settings. Pins 6 and 8 of the IE-789468-NS-EM1's socket (X2) on the parts board (X2) are shorted. Set the jumper (JP1) to 2-3 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).





Remark The clock that is supplied by the IE-789468-NS-EM1's resonator (encircled in the figure) is used.

Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the socket (X2).

(2) When using clock mounted by user

The settings of either (a) or (b) described in the following pages are required, depending on the type of clock to be used. Set the jumper (JP1) on the IE-789468-NS-EM1 to 2-3 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).





Remark The clock that is supplied by the IE-789468-NS-EM1's oscillator (encircled in the figure) is used.



Outline Diagram

Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.

(a) When using a crystal resonator

- Necessary items
- Crystal resonator
- Resistor Rx
- Parts board

- Capacitor CACapacitor CB
- Solder kit

- <Procedure>
- <1> Prepare a parts board.
- <2> Solder the target crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequencies) onto the supplied parts board as shown below.





| Pin No. | Connection |
|---------|-------------------|
| 2-13 | Capacitor CA |
| 3-12 | Capacitor CB |
| 4-11 | Crystal resonator |
| 5-10 | Resistor Rx |
| 8-9 | Shorted |

Circuit Diagram



Remark The section enclosed by dotted lines indicates the section to be mounted on the parts board. See the resonator data sheets prepared by the resonator manufacturer for details of the values for resistor Rx, capacitor CA, and capacitor CB.

- <3> Prepare the IE-789468-NS-EM1.
- <4> Remove the jumper that is mounted in the IE-789468-NS-EM1's socket (X2).
- <5> Make sure that the parts board is wired as shown in Figure 3-14 above.
- <6> Connect the parts board (from <2> above) to the socket (X2) from which the jumper was removed in <4>. Check the pin 1 mark to make sure the board is mounted in the correct direction.
- <7> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(b) When using a crystal oscillator

- Necessary items
- Crystal oscillator (with pin configuration as shown in Figure 3-15)

Figure 3-15. Crystal Oscillator (Subsystem Clock)



<Procedure>

- <1> Prepare the IE-789468-NS-EM1.
- <2> Remove the jumper from the socket (X2) on the IE-789468-NS-EM1.
- <3> Mount the crystal oscillator in the socket (X2) from which the jumper was removed in <2>. At this time, insert the crystal oscillator pin into the socket pin as indicated below.

Figure 3-16. Correspondence Between Crystal Oscillator and Socket (Subsystem Clock)



| Crystal Oscillator Pin | Socket Pin No. |
|------------------------|----------------|
| NC | 1 |
| GND | 4 |
| CLOCK OUT | 8 |
| Vcc | 14 |

<4> Install the IE-789468-NS-EM1 in the IE-78K0S-NS or IE-78K0S-NS-A.

(3) When using a pulse input from the target system

The external clock pulse signal on the target system is used via an emulation probe. Set JP1 on the IE-789468-NS-EM1 to 1-2 shorted.

There is no need to make any settings in the integrated debugger (ID78K0S-NS).



Figure 3-17. When Using Pulse Input from Target System (Subsystem Clock)



Outline Diagram



Remark The flow of the clock inside the IE-789468-NS-EM1 is indicated by the bold line.
3.6 Mask Option Settings

3.6.1 Mask option when μ PD789327 Subseries is debugged

In the IE-789468-NS-EM1, the oscillation stabilization time, which is set by a mask option in the μ PD789327 Subseries, cannot be selected. The oscillation stabilization wait time is the same as that of the flash memory version, μ PD78F9327.

• Oscillation stabilization time: 2¹⁵/fx (fixed)

3.6.2 Mask option when μ PD789327, 789467 Subseries is debugged

In the IE-789468-NS-EM1, whether to use the POC circuit, which is set by a mask option in the μ PD789327, 789467 Subseries, can be selected. The switch settings are shown in Table 3-7.

| Table 3-7. Selection of Use of POC Circuit |
|--|
|--|

| POC Circuit | SW1 | | |
|-------------------------|-----------------------|--|--|
| POC circuit is used | POC ON side (2-side) | | |
| POC circuit is not used | POC OFF side (1-side) | | |

Caution Set the switch when the power of the IE-78K0S-NS or IE-78K0S-NS-A is off.

3.7 External Trigger

To set an external trigger, connect it to the IE-789468-NS-EM1's check pin, EXTOUT pin and EXTIN pin. The input pin position is shown in Figure 3-18.

See the IE-78K0S-NS User's Manual (U13549E) or IE-78K0S-NS-A User's Manual (U15207E) for descriptions of pin characteristics.

See the ID78K Series Integrated Debugger Ver.2.30 or Later Operation User's Manual (Windows[™] Based) (U15185E) for descriptions of usage.

(1) EXTOUT

A low-level pulse is output from the IE-789468-NS-EM1's EXTOUT pin for 1.3 μ s upon the occurrence of a break event.

Caution Because this is an open-drain output, a pull-up resistor should be connected on the target system.

(1) EXTIN

An event signal can be input from the IE-789468-NS-EM1's EXTIN pin. Input a high-level pulse signal for 2 CPU operating clocks or longer.



Figure 3-18. External Trigger Input Position

CHAPTER 4 DIFFERENCES BETWEEN TARGET DEVICES AND TARGET INTERFACE CIRCUITS

This chapter describes differences in electrical characteristics between the target device and the target interface circuit.

The target interface circuit of the IE system consists of an emulation CPU, TTL, CMOS-IC, and other emulation circuits. Differences in electrical characteristics between the target device and the target interface circuit occur due to the existence of a protection circuit.

- (1) Signals directly input/output to/from the EVA chip and peripheral EVA chip
- (2) Signals input from the target system via a gate
- (3) Other signals

The circuits of the IE-789468-NS-EM1 for the signals in (1) to (3) above are shown below.

(1) Signals directly input/output to/from the EVA chip and peripheral EVA chip

Refer to Figure 4-1 Equivalent Circuit of Emulation Circuit (1).

The following signals operate in the same manner as those in the μ PD789327, 789467 Subseries.

- Signals related to port 0
- Signals related to port 1
- Signals related to port 4
- Signals related to port 6
- Signals related to port 8 (S17 to S22)
- S0 to S16
- COM0 to COM3

A pull-up resistor of 1 M Ω is directly inserted in the following signal.

• Signals related to port 2 (µPD789327 Subseries only)

Figure 4-1. Equivalent Circuit of Emulation Circuit (1)

Probe side(Target system)

♦ IE system



(2) Signals input from the target system via a gate

Since the following signals are input via a gate, their timing shows a delay compared to that of the μ PD789327, 789467 Subseries. Refer to Figure 4-2 Equivalent Circuit of Emulation Circuit (2).

- Signals related to RESET
- Signals related to clock input

The IE-789468-NS-EM1 does not use the X2 and XT2 pins.

- CAPH, CAPL (µPD789467 Subseries only)
- VLC0 to VLC2 (VLC1 and VLC2 are available in the μ PD789467 Subseries only)



Figure 4-2. Equivalent Circuit of Emulation Circuit (2)

(3) Other signals

Refer to Figure 4-3 Equivalent Circuit of Emulation Circuit (3).

• VDD pin

When the target system is not connected, the power supply of the emulation CPU operates with the internal supply voltage (5 V). When the target system is connected, it operates with the power (LVcc) supplied from the low-voltage supply pin (TM1).

The V_{DD} pin of the target system is only used to control the LED1 (USER VDD) that monitors the connection of the target system power supply in the IE-789468-NS-EM1.

Vss pin

The Vss pin is connected to GND inside the IE-789468-NS-EM1.

• IC/VPP pin

The IE-789468-NS-EM1 does not use the IC/VPP pin.



Figure 4-3. Equivalent Circuit of Emulation Circuit (3)

CHAPTER 5 CAUTIONS

This chapter describes differences between the target device and the IE system specifications.

The emulation circuit of the IE system consists of an EVA chip, TTL, CMOS-IC, and other circuits. Therefore, there are differences between the target device and the IE system specifications.

• Read value of port 2 when the target system is not connected

Port 2 of the μ PD789327 Subseries is directly connected to a 1 M Ω pull-up resistor. When the port value is read in input mode when the target system is not connected, the value read from port 2 is 07h.

• Oscillation stabilization wait time cannot be changed

The oscillation stabilization wait time of the μ PD789327 Subseries (mask ROM version) after STOP mode is released by RESET input or power-on clear is the same as that of the μ PD78F9328 (flash memory version).

• 2¹⁵/fx (fixed)

APPENDIX A EMULATION PROBE PIN ASSIGNMENT TABLE

| Emulation Probe Pin No. | CN1 Pin No. | Emulation Probe Pin No. | CN1 Pin No. |
|----------------------------|-------------|----------------------------|-------------|
| 1 | 118 | 31 | 22 |
| 2 | 114 | 32 | 28 |
| 3 | 108 | 33 | 92 |
| 4 | 104 | 34 | 91 |
| 5 | 100 | 35 | 98 |
| 6 | 94 | 36 | 102 |
| 7 | 30 | 37 | 106 |
| 8 | 29 | 38 | 112 |
| 9 | 24 | 39 | 116 |
| 10 | 20 | 40 | 87 |
| 11 | 16 | 41 | 83 |
| 12 | 10 | 42 | 77 |
| 13 | 6 | 43 | 73 |
| 14 | 33 | 44 | 69 |
| 15 | 37 | 45 | 63 |
| 16 | 43 | 46 | 61 |
| 17 | 47 | 47 | 65 |
| 18 | 51 | 48 | 71 |
| 19 | 57 | 49 | 75 |
| 20 | 59 | 50 | 79 |
| 21 | 55 | 51 | 85 |
| 22 | 49 | 52 | 89 |
| 23 | 45 | | |
| 24 | 41 | | |
| 25 | 35 | | |
| 26 | 31 | | |
| 27 | 4 | | |
| 28 | 8 | | |
| 29 | 14 | | |
| 30 | 18 | | |

Table A-1. Pin Assignment of NP-H52GB-TQ

Remark NP-H52GB-TQ is a product of Naito Densei Machida Mfg. Co., Ltd.

APPENDIX B CAUTIONS ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the emulation probe, conversion connector, and conversion socket. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.





