CUSTOMER NOTIFICATION

SUD-DT-03-0180-4-E (1/4)
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IE-780959-NS-EM1
(Control Code C)
Operating Precautions

Be sure to read this document before using the product.

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Notes on Using IE-780959-NS-EM1

1. Product Version

Product name: IE-780959-NS-EM1

Control Code[Note]	Remark
A	
B	
C	

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]		
		A	B	C
1	Bug in D/A converter output pin	×	√	√
2	Bug in clock generator (1)	×	√	√
3	Bug in clock generator (2)	×	×	√
4	Bug in clock generator (3)	×	×	√

×: Applicable, √: Not applicable or already corrected

3. Details of Bugs and Added Specifications

No.1 Bug in D/A converter output pin

[Description]

When D/A converter operation is stopped (DACE0n = 0), a low level is output from the ANOn pin (n = 0 or 1).

[Workaround]

There is no workaround.

[Correction]

This bug has been corrected in control code B.

No.2 Bug in clock generator (1)

[Description]

Noise is superimposed on the clock signal when switching main system clock 1 and 2 (MCKS setting), which causes the IE system to malfunction.

[Workaround]

There is no workaround.

[Correction]

This bug has been corrected in control code B.

No.3 Bug in clock generator (2)

[Description]

When the division ratio (MPRS) of the main system clock is set while the CPU is operating on f_{XT} (f_{CC1}: Oscillation stop, f_{X2}: Oscillation stop), and then f_{CC1} is set to “oscillation” (MCC = 0) or f_{X2} to “oscillation” (CKC2 = 1), the value of MPRS becomes illegal. (The correct value of MPRS cannot be read.)

f_{CC1}: Main system clock 1

f_{X2}: Main system clock 2

f_{XT}: Subsystem clock

[Workaround]

When the CPU is operating on f_{XT}, set f_{CC1} to “oscillation” (MCC = 0) or f_{X2} to “oscillation” (CKC2 = 1) before setting the division ratio (MPRS) of the main system clock.

[Correction]

This bug has been corrected in control code C.

No.4 Bug in clock generator (3)

[Description]

When a debug operation is performed while f_{XT} is used as the CPU clock and f_{CC1} and f_{X2} are stopped, the integrated debugger hangs up upon a break.

f_{CC1}: Main system clock 1

f_{X2}: Main system clock 2

f_{XT}: Subsystem clock

[Workaround]

Always keep f_{CC1} or f_{X2} in the “oscillation” status (f_{CC1} oscillation: MCC = 0, f_{X2} oscillation: CKC2 = 1)

[Correction]

This bug has been corrected in control code C.

4. Cautions

4.1 Restrictions

No.1 The integrated debugger may not be activated.

When activating the integrated debugger, an error message is displayed and the debug screen may not appear.

[Workaround]

Press the reset button on the IE-780959-NS-EM1 to restart the debugger.

No.2 The port pins are pulled up at the following voltage between when power is applied to the IE system and when the ID78K0-NS is activated (the debug screen is displayed).

When the target system power supply is off: 3.3 V

When the target system power supply is on: 5.0 V

[Workaround]

There is no workaround.

No.3 Up to 1 μA of leakage current flows through the mask option pins (RESET_B, P60, and P110) even if no pull-up resistor is connected. At this time, the input initial value of P60 and P110 is undefined.

[Workaround]

There is no workaround.

No.4 Clock settings

Clock settings are performed using a combination of JP1 of the IE-780959-NS-EM1 and the integrated debugger (ID78K0-NS) (see the IE-780959-NS-EM1 User's Manual for details).

The IE system hangs up if a prohibited setting is made.

Clock Settings	Integrated Debugger (ID78K0-NS)	IE-780959-NS-EM1 JP1
Main system clock 1: Clock on CL1 Main system clock 2: Clock on X1	Internal clock (Internal)	1-2 shorted
Setting prohibited	Internal clock (Internal)	2-3 shorted
Setting prohibited	External clock (External)	1-2 shorted
Main system clock 1: Clock on UCL1 Main system clock 2: Clock on the target system	External clock (External)	2-3 shorted

4.2 Cautions

Use the IE-78K0-NS (control code L or later) or IE-78K0-NS-A (control code E or later). Even if using the product with the latest control code, emulation cannot be performed correctly (the integrated debugger may hang up) when used in combination with IE-78K0-NS control code A to C.

NEC Electronics will provide separate support for IE-78K0-NS control code A to C, so please contact an NEC Electronics sales representative or distributor.

The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.