CUSTOMER NOTIFICATION

SUD-DT-03-0119-3 (1/9)

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IE-780148-NS-EM1

(Control Code: A, B, C, D, E)

Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-780148-NS-EM1

1. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code[Note]				
		A	B	C	D	E
1	Read value of SFR register RESF is illegal.	×	√	√	√	√
2	Oscillation stabilization time differs from that of target device.	×	√	√	√	√
3	LVI reset generation function does not operate correctly.	×	√	√	√	√
4	Emulation at operating voltage of 4.0 V or below is impossible.	×	√	√	√	√
5	LED2 (POC RESET) to indicate POC reset has been added [Addition of specification]	–	√	√	√	√
6	The integrated debugger ID78K0-NS hangs up if break is inserted after SFR register MSTOP is set to 1	×	×	√	√	√
7	When masking is specified for the Ring-OSC mask option, selection of watchdog timer operating clock differs from that in the target device.	×	×	√	√	√
8	The IE system cannot be activated when Break is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS	×	×	√	√	√
9	The integrated debugger ID78K0-NS may not be able to be activated.	×	×	√	√	√
10	The value of the ADCR register is illegal when the PCC register is set to 00H or 40H	×	×	√	√	√
11	The long-type emulation probe 80-pin package (NP-H80GC-TQ and NP-H80GK-TQ) cannot be used	×	×	√	√	√
12	SFRs may not be able to be accessed ~~when operating at a frequency of over 5 MHz and at 2.7 to 4.5 V~~	×	×	×	×	√
13	Transmit data cannot be written to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1	×	×	×	√	√
14	The timing to switch the Ring-OSC and main system clock differs from that in the target device	–	–	√	√	√
15	LED3 (RETRY) to indicate the wait (retry) status has been added [Addition of specification]	–	–	√	√	√
16	Read value of the multiplication/division data register MDB0 may be illegal.	×	×	×	√	√
17	An internal reset may not be generated by the watchdog timer	×	×	×	√	√
18	The integrated debugger may not start when it is restarted	×	×	×	×	√
19	Some 78K0/Kx1+ functions are now supported [Addition of specification]	–	–	–	–	√

×: Applicable, √: Not applicable (addition of specifications), –: Specifications not supported

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased. If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Details of Bugs and Added Specifications

No.1 Read value of SFR register RESF is illegal.

[Description]

The read value of the SFR register RESF is illegal

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.2 Oscillation stabilization time differs from that of target device.

[Description]

The oscillation stabilization time differs from that of the target device.

	Target Device	IE System
After reset	17 clocks of Ring-OSC	0 [s]
After STOP mode release	Time set by the OSTS register	0 [s]

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.3 LVI reset generation function does not operate correctly.

[Description]

The LVI reset generation function (setting the SFR register LVIMD to 1) does not operate correctly.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.4 Emulation at operating voltage of 4.0 V or below is impossible.

[Description]

Emulation at an operating voltage of 4.0 V or below is impossible.

[Workaround]

There is no workaround. This bug has been corrected in control code B.

No.5 LED2 (POC RESET) to indicate POC reset has been added [Addition of specification]

[Description]

LED2 (POC RESET), which indicates a POC reset, has been provided in control code B.

LED2 is lit during the reset shown below. Do not perform a break when LED2 is lit; otherwise the integrated debugger ID78K0-NS will hang up.

- Internal reset by comparing the power supply voltage and detection voltage of the POC circuit
- Internal reset by comparing the power supply voltage and detection voltage of the low-voltage detector (LVI)
- Clock monitor reset by pressing emulation switch SW2 on the clock monitor

No.6 The integrated debugger ID78K0-NS hangs up if break is inserted after SFR register MSTOP is set to 1

[Description]

The debugger hangs up if a break is inserted after the SFR register MSTOP is set to 1.

[Workaround]

There is no workaround. This bug has been corrected in control code C.

No.7 When masking is specified for the Ring-OSC mask option, selection of watchdog timer operating clock differs from that in the target device.

[Description]

When masking is specified for the Ring-OSC mask option, selection of the watchdog timer operating clock differs from that in the target device.

Target device: Only the Ring-OSC clock is selected.

IE system: The Ring-OSC clock, X1 input clock, or watchdog timer operation stop can be selected.

[Workaround]

There is no workaround. This bug has been corrected in control code C.

No.8 The IE system cannot be activated when Break is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS

[Description]

The IE system cannot be activated when Break is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS (there is no problem when Non Break is specified.)

Consequently, the peripheral functions cannot be stopped at a break.

[Workaround]

There is no workaround. This bug has been corrected in control code C, but restrictions No.6 and 7 are still applicable.

No.9 The integrated debugger ID78K0-NS may not be able to be activated

[Description]

The integrated debugger ID78K0-NS may not be able to be activated.

[Workaround]

There is no workaround. This bug has been corrected in control code C.

No.10 The value of the ADCR register is illegal when the PCC register is set to 00H or 40H

[Description]

The value of the ADCR register is illegal when the PCC register is set to 00H or 40H.

[Workaround]

There is no workaround. This bug has been corrected in control code C.

No.11 The long-type emulation probe 80-pin package (NP-H80GC-TQ and NP-H80GK-TQ) cannot be used

[Description]

The long-type emulation probe 80-pin package (NP-H80GC-TQ and NP-H80GK-TQ) cannot be used.

[Workaround]

There is no workaround. This bug has been corrected in control code C.

No.12 SFRs may not be able to be accessed ~~when operating at a frequency of over 5 MHz and at 2.7 to 4.5 V~~

[Description]

- When using a product with control code A to C, SFRs may not be able to be accessed when operating at the following frequency and voltage.

Voltage	Frequency
2.7 to 4.5 V	Over 5 MHz

- When using a product with control code D, SFRs may not be able to be accessed when operating at the following frequency and voltage.

Voltage	Frequency
3.3 V ≤ V_{DD} < 4.5 V	Over 7 MHz

[Workaround]

There is no workaround. This bug will be corrected in control code E or later.

No.13 Transmit data cannot be written to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1

[Description]

When writing transmit data to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0) of the target device 78K0/KF1, data may not be written correctly depending on the instruction executed after the write instruction (see SBG-DT-0128-E for details).

[Workaround]

See [Workaround] (3) in SBG-DT-0128-E.

This restriction has been corrected in control code D.

No.14 The timing to switch the Ring-OSC and main system clock differs from that in the target device.

[Description]

The timing to switch the Ring-OSC and main system clock differs from that in the target device.

	Maximum Time Required for Switching	
	Main System Clock to Ring-OSC	Ring-OSC to Main System Clock
Target device	Time specified in the manual of each target device	Time specified in the manual of each target device
IE system	4f_X **Note**	Time specified in the manual of each target device + f_X **Note**

Note fx: Main system clock operating frequency

[Workaround]

There is no workaround. This restriction has been corrected in control code C.

No.15 LED3 (RETRY) to indicate the wait (retry) status has been added [Addition of specification]

[Description]

LED3 (RETRY), which indicates the wait (retry) status, has provided in control code C.

No.16 Read value of the multiplication/division data register MDB0 may be illegal.

[Description]

The read value of the multiplication/division data register MDB0 may be illegal.

[Workaround]

There is no workaround. This restriction has been corrected in control code D.

No.17 An internal reset may not be generated by the watchdog timer

[Description]

An internal reset may not be generated by the watchdog timer.

[Workaround]

There is no workaround. This restriction has been corrected in control code D.

No.18 The integrated debugger may not start when it is restarted

[Description]

The integrated debugger may not start after it is shut down and restarted.

[Workaround]

Be sure to disconnect the power supply to the IE-78K0-NS or IE-78K0-NS-A after the integrated debugger is shut down. This restriction has been corrected in control code E.

No.19 Some 78K0/Kx1+ functions are now supported. [Addition of specification]

[Description]

Some 78K0/Kx1+ functions are now supported in control code E, but restrictions apply.

See No.8 in **3. Restrictions** for details.

3. Restrictions

No.1 The initial value of the SFR PCC differs between the target device and IE system.

[Description]

The initial value of the SFR PCC differs between the target device and IE system.

Target device: 00H IE system: 04H

[Workaround]

Set 00H when the target device is started or reset.

No.2 The handling of the $\overline{\text{RESET}}$ pin differs from that in the target device.

[Description]

The handling of the $\overline{\text{RESET}}$ pin differs from that in the target device.

Target device: Without pull-up IE system: 4.7 kΩ pull-up in the IE system

[Workaround]

There is no workaround.

Correction is planned in line with upgrading the integrated debugger ID78K0-NS.

<<Permanent restriction>>

No.3 The values of the RESF, LVIM, and LVIS registers are initialized by applying a reset from the target system even if RESET is masked

[Description]

The values of the RESF, LVIM, and LVIS registers are initialized by applying a reset from the target system to the IE system even if RESET is masked in the Configuration dialog box of the integrated debugger ID78K0-NS. (The values of other registers are not initialized.)

[Workaround]

There is no workaround.

No.4 The values of the RESF, LVIM, and LVIS registers are not initialized by the CPU reset button of the integrated debugger ID78K0-NS.

[Description]

The values of the RESF, LVIM, and LVIS registers are not initialized by the CPU reset button of the integrated debugger ID78K0-NS.

[Workaround]

Initialization can be implemented using the following resets.

<RESF register>

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage

<LVIM and LVIS registers>

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage
- Clock monitor reset by pressing emulation switch SW2 on the clock monitor
- Reset applied from the watchdog timer

No.5 Do not use an accessing method that generates a wait request for the WDTM, ASIS0, ASIS6, ADM, ADS, PFM, PFT, and ADCR registers when operating with the subsystem clock and with the input clock stopped

[Description]

Do not use an accessing method that generates a wait request for the WDTM, ASIS0, ASIS6, ADM, ADS, PFM, PFT, and ADCR registers when operating with the subsystem clock and with the input clock stopped.

[Workaround]

LED3 (RETRY) stays lit in the IE system, the integrated debugger ID78K0-NS hangs up. Apply a reset by using either of the following methods to restore from the hang-up status.

- Reset applied from a circuit on the target device
- Internal reset by comparing the power supply voltage of the POC circuit and detection voltage
- Internal reset by comparing the power supply voltage of the low-voltage detector (LVI) and detection voltage
- Clock monitor reset by pressing emulation switch SW2 on the clock monitor

No.6 The value of the A/D conversion result register (ADCR) in the SFR window and Watch window is illegal when the peripheral functions are set to be stopped

[Description]

The value of the ADCR register in the SFR window and Watch window is illegal when Break (peripheral functions stopped) is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS (there is no problem when Non Break is specified. In addition, there is no problem with the read value in the program.)

[Workaround]

There is no workaround.

No.7 Values may not be able to be written to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers in the SFR window and Watch window when the peripheral functions are set to be stopped

[Description]

Values may not be able to be written to the TMC00, TMC01, WDTM, ADM, ADS, PFM, and PFT registers in the SFR window and Watch window when Break (peripheral functions stopped) is specified as Peripheral Break in the Configuration dialog box of the integrated debugger ID78K0-NS (there is no problem when Non Break is specified. In addition, there is no problem with write in the program.)

[Workaround]

There is no workaround.

No.8 Restrictions on using 78K0/Kx1+

[Description]

(1) Accessing bits 7, 6, 2, 1, and 0 of the memory expansion mode register (MM) and the system control register (VSWC) is not possible.

(2) An operating voltage lower than 2.5 V is not supported.
The POC function generates an internal reset signal when the voltage becomes 2.1 ±0.1 V.
The LVI function does not support a detection voltage (VLVI) of 2.35 V ±0.1 V.

(3) The self-programming function is not supported.

(4) The boot swap function is not supported.

(5) An operating frequency of 16 MHz max. is not supported.
The maximum operating frequency varies depending on the conditions shown below. The frequencies lower than maximum operating frequency are the same as those of the device specifications.

IE-78K0-NS-A	Control code E, F:	10 MHz max. (4.0 V ≤ V_{DD} ≤ 5.5 V)
IE-78K0-NS-A	Control code G or later:	12 MHz max. (4.0 V ≤ V_{DD} ≤ 5.5 V)
IE-78K0-NS	Control code L, M:	10 MHz max. (V_{DD} = 5.0 V)
IE-78K0-NS	Control code n or later:	10 MHz max. (4.0 V ≤ V_{DD} ≤ 5.5 V)
IE-78K0-NS	Control code N or later:	12 MHz max. (4.0 V ≤ V_{DD} ≤ 5.5 V)

(6) The option byte function is not supported. Set RINGOSC using the mask option of the debugger.

[Workaround]

There is no workaround.

4. Cautions

No.1 Use the IE-78K0-NS (control code L or later) or IE-78K0-NS-A (control code E or later). Even if using the product with the latest control code, emulation cannot be performed correctly (the integrated debugger may hang up) when used in combination with IE-78K0-NS control code A to C.

NEC Electronics will provide a special upgrade for IE-78K0-NS control code A to C, so please contact an NEC Electronics sales representative or distributor in this case.
After upgrade, the control code is n (equivalent to control code N).

The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.