CUSTOMER NOTIFICATION

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Koji Nishibayashi, Senior System Integrator
Microcomputer Group
2nd Solutions Division
Solutions Operations Unit
NEC Electronics Corporation

CP(K), O

IE-703166-MC-EM1

Preliminary User's Manual

(2nd Edition)

CONTENTS

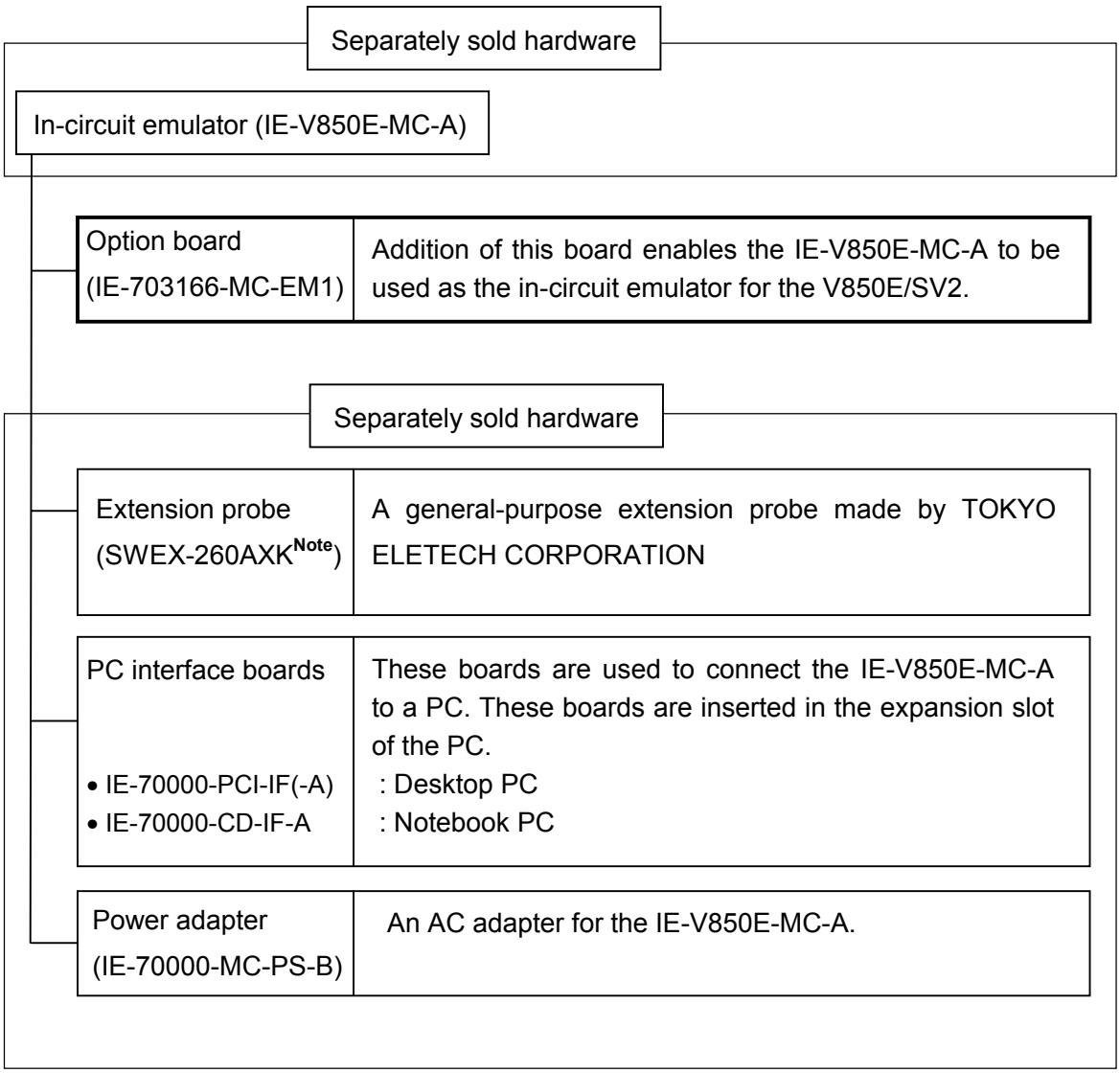
CHAPTER 1 OVERVIEW

The IE-703166-MC-EM1 is an option board for the in-circuit emulator IE-V850E-MC-A. By connecting the IE-V850E-MC-A, the IE-703166-MC-EM1 can effectively debug hardware or software in system development using the V850E/SV2.

This manual explains the basic setup procedure, hardware specifications, system specifications, and settings for the switches.

Refer to the IE-V850E-MC, IE-V850E-MC-A User's Manual (U14487E) for details of the names and functions of each block in the IE-V850E-MC-A and connection with the components.

1.1 Product Configuration



Note For further information, contact: Daimaru Kogyo, Ltd.

Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)

1.2 Hardware Specifications (When Connected to IE-V850E-MC-A)

Table 1-1. Hardware Specifications

Parameter		Specification	
Target device		μPD70(F)3166(Y)	
Target board interface voltage		VDD	2.3 to 2.7 V
		EVDD	2.7 to 3.6 V
		CVDD	2.7 to 3.6 V
		PVDD	2.3 to 2.7 V
		AVDD	2.7 to 3.6 V
Maximum operating frequency		40.5 MHz	
External dimensions	Height	35 mm	
	Width	200 mm	
	Length	75 mm	
Power consumption		11 W	
Weight		300 g	

Compatibility with the target device is enhanced by eliminating buffers between signal lines.

8-bit external trace possible by connecting to the external logic probe (attached).

The following pins can be masked.

RESET, NMI, WAIT, HLDRQ

1.3 IE-703166-MC-EM1 System Specifications (When Connected to IE-V850E-MC-A)

Table 1-2. IE-703166-MC-EM1 System Specifications (When Connected to IE-V850E-MC-A)

Parameter		Specification
Emulation memory capacity	Internal ROM	1 MB MAX.
	External memory	4 MB MAX.
Program execution function	Real-time execution function	Go, Start, Go & Go, Come, Restart, Return out
	Non-real-time execution function	Step-in, next over, slowmotion
Break function		Event detection break, software break, forced break, break by Come function, break on satisfaction of condition during step execution, Fail-safe break
Trace function	Trace condition	All trace, section trace, qualify trace
	Memory capacity	168 bits × 32K frames
Other functions		Mapping function, event function, coverage measurement function, snapshot function, stub function, register manipulation function, memory manipulation function, time measurement function, real-time RAM sampling function

Caution Some functions may not be supported, depending on the debugger used.

1.4 System Configuration

The following shows the system configuration when using the IE-703166-MC-EM1 connected to the IE-V850E-MC-A and a PC (PC-9800 series or PC/AT compatible).

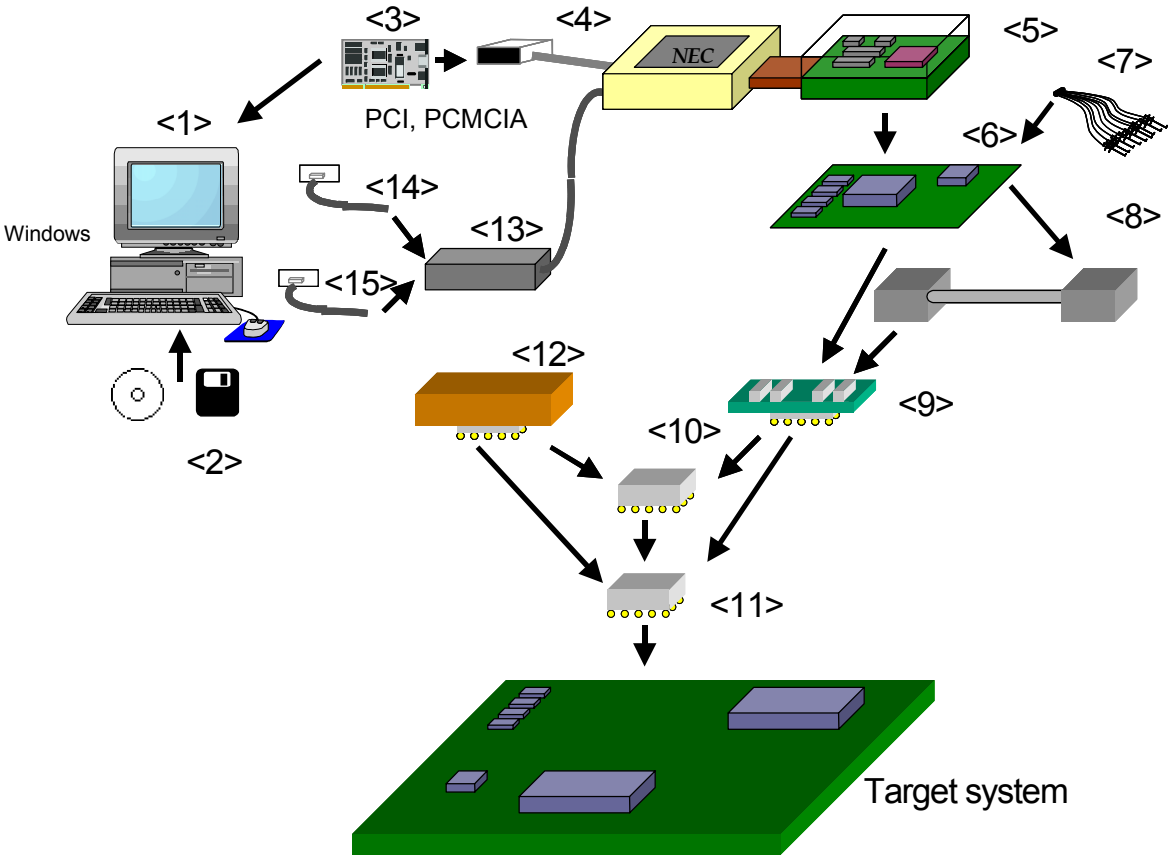


Figure 1-1. System Configuration

<1> Host machine (PC-9800 series, IBM PC/AT compatible)

<2> Debugger (sold separately), device file (separately available)

<3> PC interface board (IE-70000-PCF-IF(-A), IE-70000-CD-IF-A: sold separately)

<4> PC interface cable (included with IE-V850E-MC-A)

<5> In-circuit emulator (IE-V850E-MC-A: sold separately)

<6> In-circuit emulator option board (IE-703166-MC-EM1)

<7> External logic probe (included)

<8> Extension probe (optional) (SWEX-260AKX: sold separately)

<9> Emulator connector (CSICE257B2014N01: included)

<10> Mounting spacer (optional) (CSSOCKET257B2014N01: sold separately)

<11> Target connector socket (BSSOCKET257B2014N01: included)

<12> Device mounting adapter (LSPACK257B2014N01: sold separately)

<13> Power supply adapter (IE-70000-MC-PS-B: sold separately)

<14> AC 220 V power supply cable (included with IE-70000-MC-PS-B)

<15> AC 100 V power supply cable (included with IE-70000-MC-PS-B)

1.5 Package Contents

The IE-703166-MC-EM1 contains the following items. Please check that all the items are included. If any items are missing or damaged, contact an NEC sales representative or distributor.

(1) IE-703166-MC-EM1:	1
(2) Warranty:	1
(3) Package details:	1
(4) Accessory list:	1
(5) External logic probe:	1
(6) Target connector socket (BSSOCKET257B2014N01):	1
(7) Emulator connector (CSICE257B2014N01):	1
(8) User's manual (this document):	1

1.6 Connection Between IE-V850E-MC-A and IE-703166-MC-EM1

The procedure for connecting the IE-V850E-MC-A and IE-703166-MC-EM1 is shown below.

Caution Be careful not to break or bend the connector pins.

(1) Remove the cover (bottom) of the IE-V850E-MC-A pod.
(2) Set the PGA socket lever of the IE-703166-MC-EM1 board to the OPEN position shown in Figure 1-3.
(3) Connect the IE-703166-MC-EM1 to the PGA socket at the back of the pod (see Figure 1-4).
Align the IE-V850E-MC-A and IE-703166-MC-EM1 horizontally.
A spacer can be mounted to fix the pod.
(4) Set the PGA socket lever of the IE-703166-MC-EM1 board to the CLOSE position shown in Figure 1-3.
(5) Fix the pod cover (bottom) to the bottom of the IE-703166-MC-EM1 using the nylon rivets provided with the IE-V850E-MC-A.

Figure 1-2. Connection of IE-V850E-MC-A and IE-703166-MC-EM1

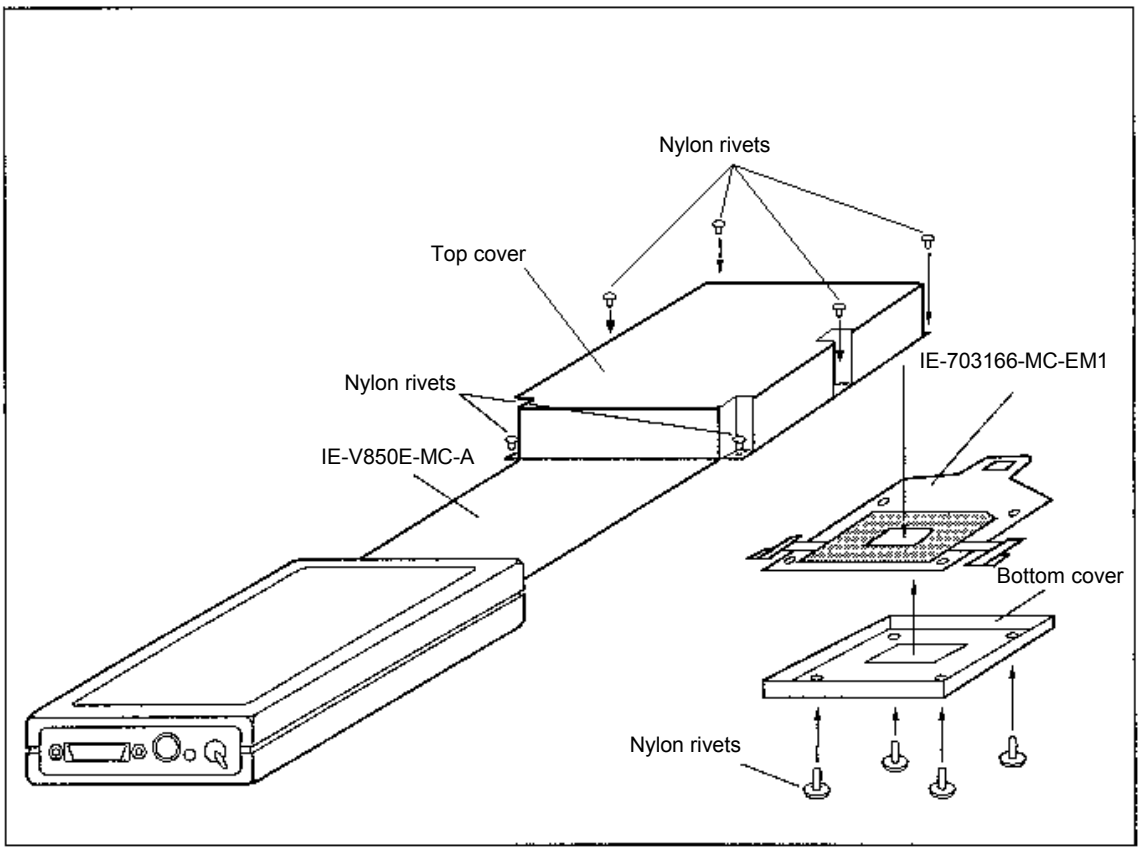


Figure 1-3. IE-703166-MC-EM1 PGA Socket Lever

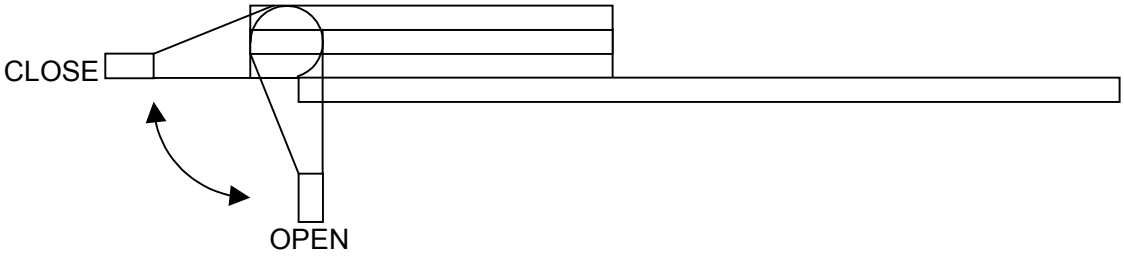
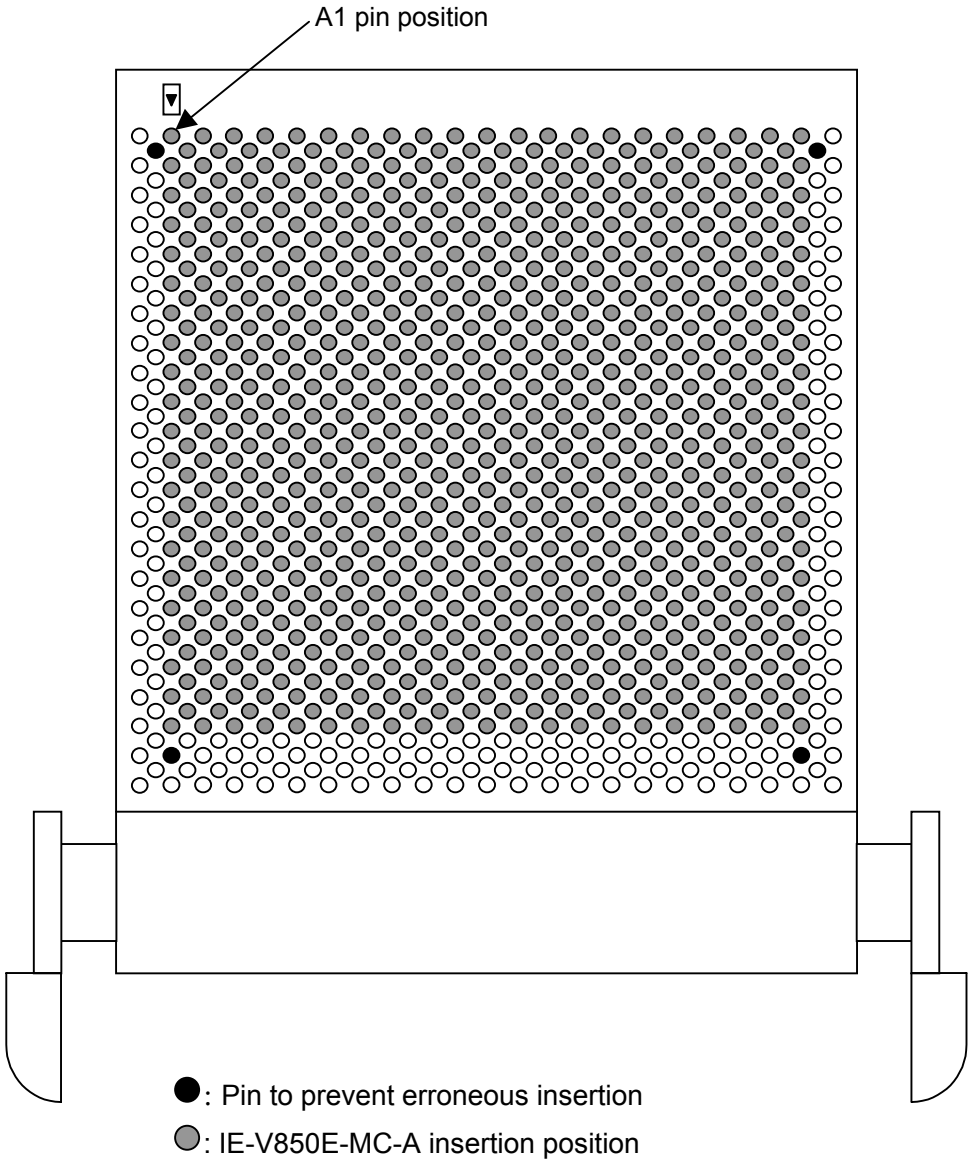


Figure 1-4. IE-V850E-MC-A Insertion Position



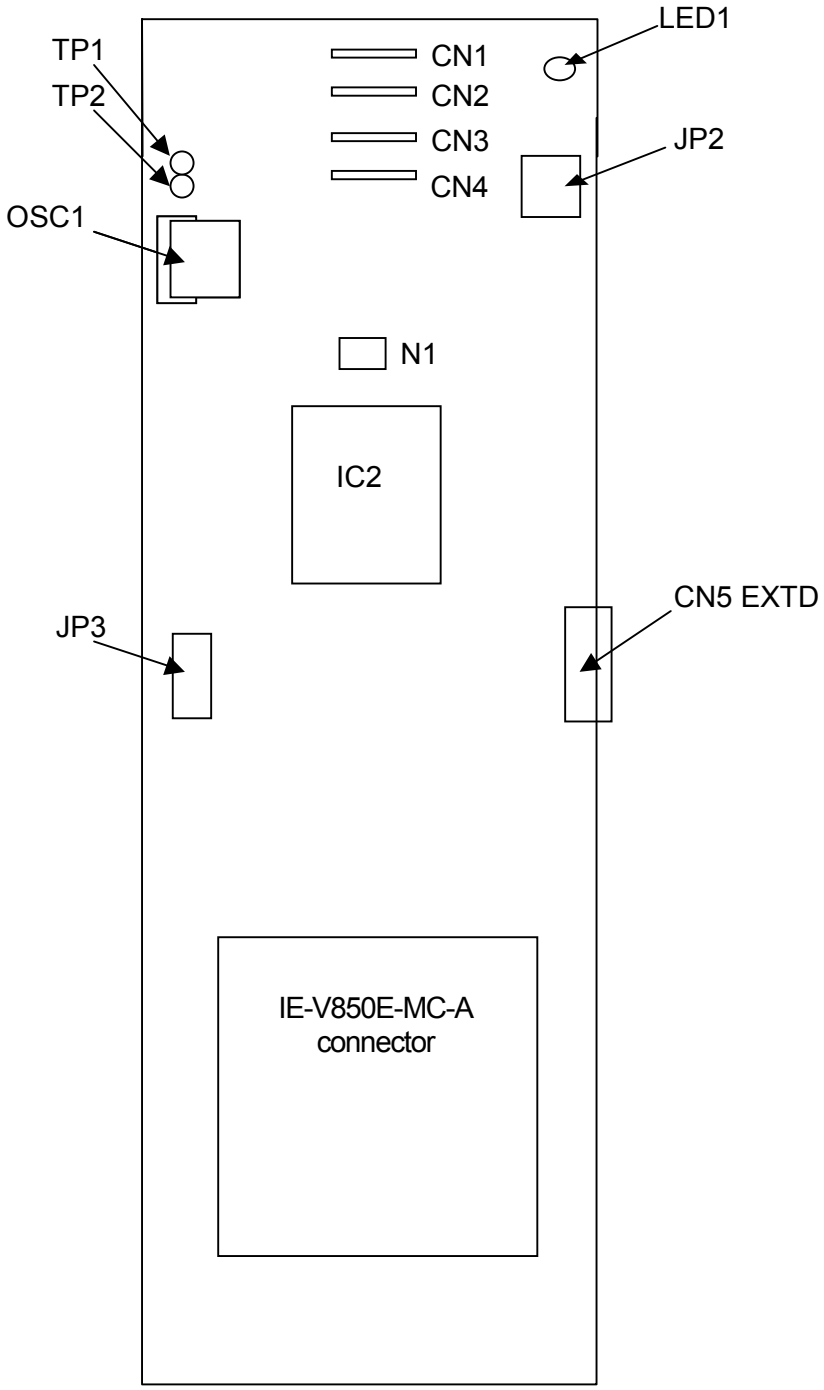
CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS

This chapter explains the names and functions of the IE-703166-MC-EM1 components and the settings for the switches.

Refer to the **IE-V850E-MC, IE-V850E-MC-A User's Manual (U14487E)** for details of the pod, the jumpers, and the switch positions.

2.1 Names and Functions of IE-703166-MC-EM1 Components

Figure 2-1. IE-703166-MC-EM1 Top View



(1) TP1, TP2

These pins are used to monitor waveforms.

- TP1: Test pin for shipment test
- TP2: GND pin

(2) OSC1

This pin is used to mount the oscillator to be used when selecting the internal clock. A 40.5 MHz crystal oscillator is mounted at shipment. (Refer to **2.2 Clock Settings** for details).

(3) CN1, CN2, CN3, CN4

These pins are used to connect the emulator connector (CSICE257B2014N01) or extension probe (SWEX-260AKX).

(4) LD2 (RUN: yellow)

This is an LED that indicates the operating status of the emulator.

LED Status	Emulator Status
Lit	User program is under execution
Extinguished	User program is stopped

(5) JP2

This is a jumper used to set the V_{DD} and EV_{DD} power supplies. (Refer to **2.3 Power Supply Settings** for details).

(6) JP3

This is a jumper used to set the AV_{DD} and AV_{REF} power supplies. (Refer to **2.3 Power Supply Settings** for details).

(7) N1

This is a screw to connect the GND of the probe when the extension probe (SWEX-260AKX) is used. (Refer to the manual of the probe (SWEX-260AKX) for details.)

(8) IC2

The I/O chip (μPD70F3166) is connected to this pin.

(9) CN5 EXTD

This is a connector used to connect the external logic probe.

(10) IE-V850E-MC-A connector

This is used to connect the IE-V850E-MC-A.

2.2 Clock Settings

2.2.1 Overview of clock settings

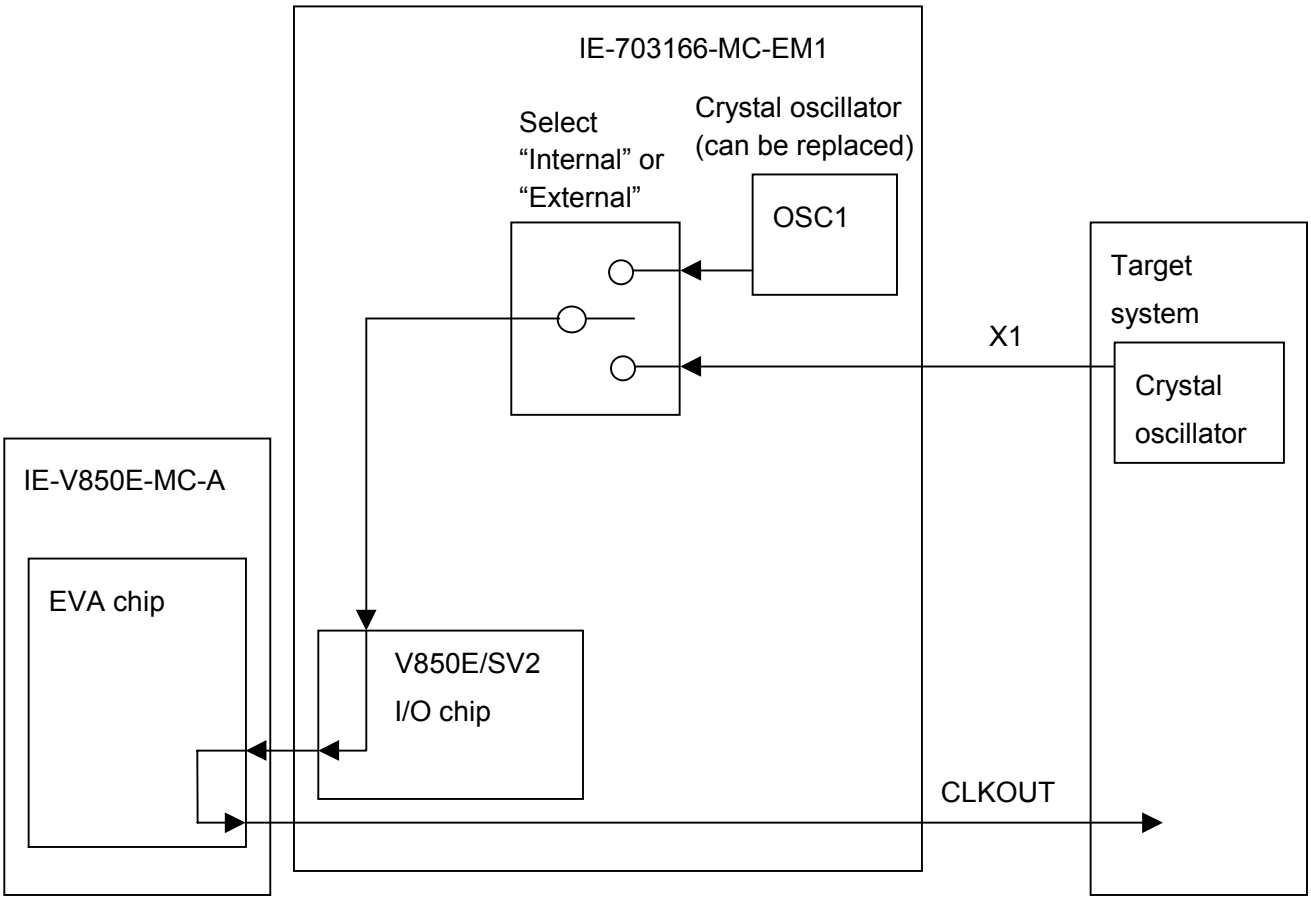
The following three clock setting methods are available. Refer to **2.2.2 Clock setting method** for details.

(1) Use the crystal oscillator that is already mounted on the IE-703166-MC-EM1 as an internal clock

(2) Replace the crystal oscillator that is already mounted on the IE-703166-MC-EM1 with a different oscillator and use that as an internal clock

(3) Use the crystal oscillator on the target system as an external clock

Figure 2-2. Overview of Clock Settings



Cautions 1. Input a square waveform to X1 when using an external clock. The board does not operate when a crystal or ceramic resonator is used.

2. The PLL cannot be used in the emulator. The through-clock mode is always selected (CKSEL1: 1).

3. The CKSEL1 and PLLSEL pins cannot be emulated.

2.2.2 Clock setting method

The hardware settings corresponding to the clock settings are listed below.

Table 2-1. Hardware Settings Corresponding to Clock Settings

Type of Clock Used	Selection of Clock Source[Note]	OSC1 Crystal Oscillator
Crystal oscillator already mounted on IE-703166-MC-EM1 used as internal clock	Internal	Factory setting (40.5 MHz)
Crystal oscillator already mounted on IE-703166-MC-EM1 replaced with different oscillator used as internal clock	Internal	Replaced
Crystal oscillator on target system used as external clock	External	Whether or not to mount a crystal oscillator can be selected

Note Select the clock source in the clock source selection area in the Configuration dialog box of the integrated debugger (ID850).

Caution Settings other than those above are prohibited.

(1) Use the crystal oscillator that is already mounted on the IE-703166-MC-EM1 as an internal clock

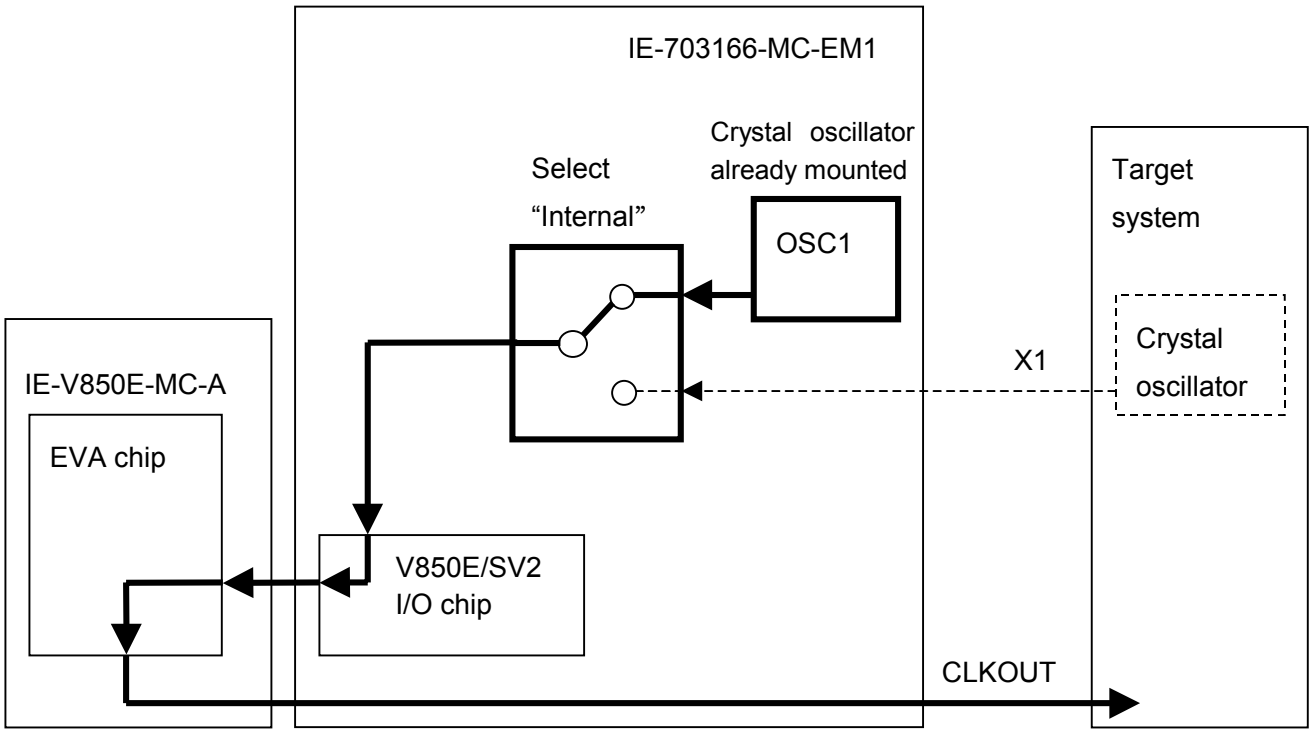
<1> Mount the 40.5 MHz crystal oscillator mounted at shipment in the OSC1 socket of the IE-703166-MC-EM1 (default setting).

<2> When the integrated debugger (ID850) is activated, select “Internal” in the clock source selection area in the Configuration dialog box (selection of the clock in the emulator).

Table 2-2. Settings When Using Crystal Oscillator Already Mounted as Internal Clock

Type of Clock Used	Selection of Clock Source	OSC1 Crystal Oscillator
Crystal oscillator already mounted on IE-703166-MC-EM1 used as internal clock	Internal	Factory setting (40.5 MHz)

Figure 2-3. Overview of Settings When Mounted Internal Clock Is Used



(2) Replace the crystal oscillator that is already mounted on the IE-703166-MC-EM1 with a different oscillator and use that as an internal clock

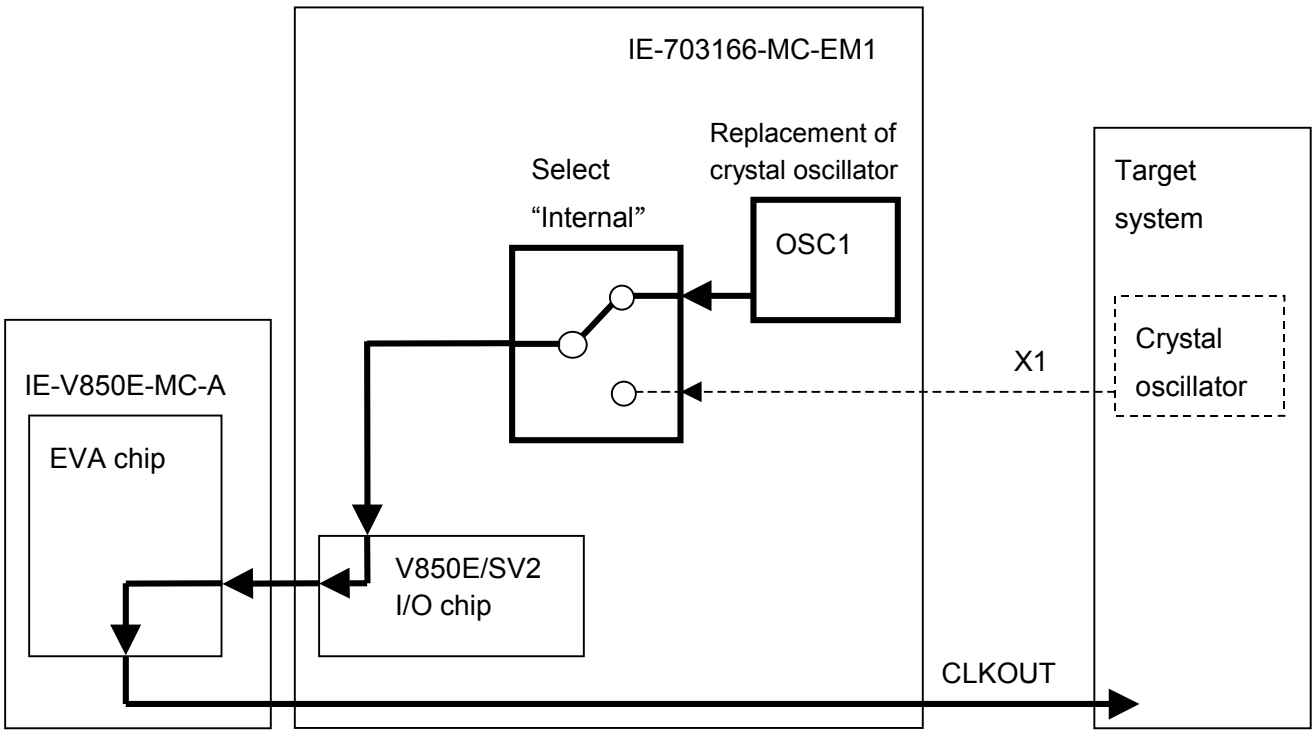
<1> Remove the crystal oscillator (OSC1) that is already mounted on the option board and mount the oscillator to be used.

<2> Select “Internal” in the clock source selection area in the Configuration dialog box of the integrated debugger (ID850)

Table 2-3. Settings When Replacing Clock Already Mounted

Type of Clock Used	Selection of Clock Source	OSC1 Crystal Oscillator
Crystal oscillator already mounted on IE-703166-MC-EM1 replaced with different oscillator used as internal clock	Internal	Replaced

Figure 2-4. Overview of Settings When Replacement Internal Clock Is Used



(3) Use the oscillator on the target system as an external clock

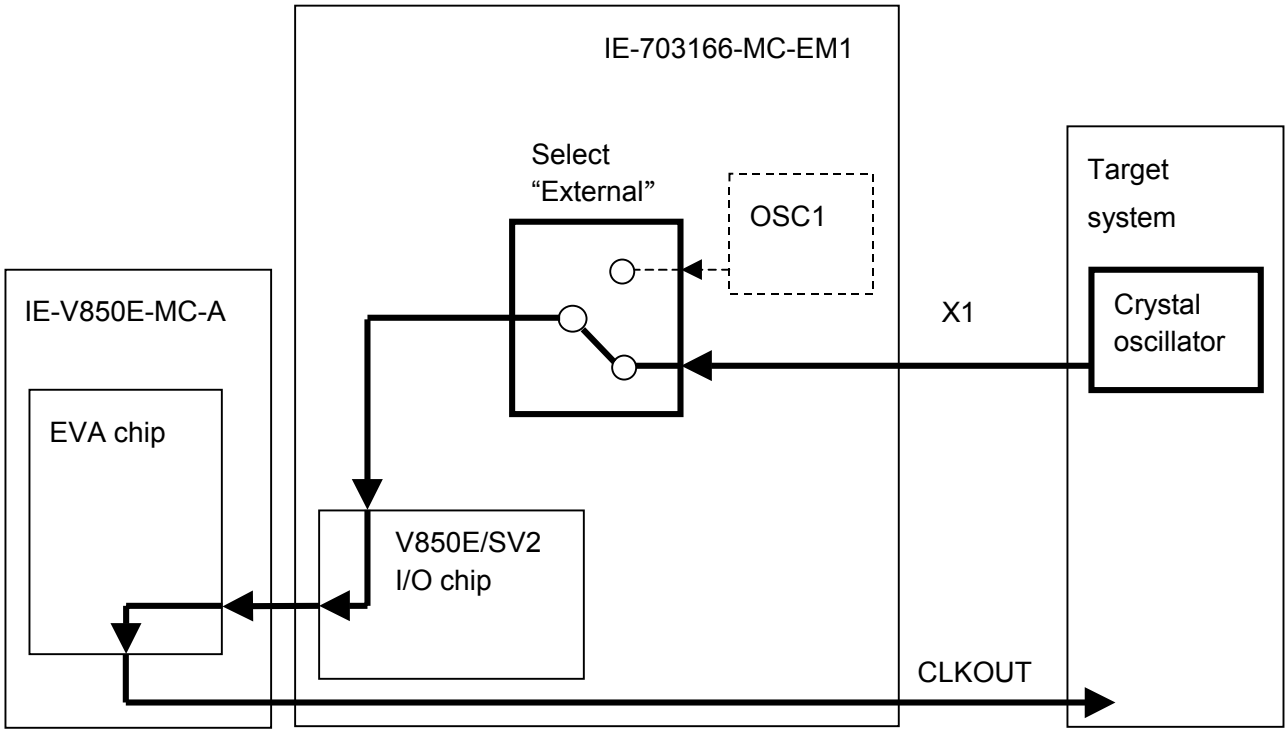
<1> Select “External” in the clock source selection area in the Configuration dialog box of the integrated debugger (ID850)

Table 2-4. Settings When Using External Clock on Target System

Type of Clock Used	Selection of Clock Source	OSC1 Crystal Oscillator
Oscillator on target system used as external clock	External	Whether to mount a crystal oscillator or not can be selected

Caution Input a square waveform to X1 when using an external clock.
The board does not operate when a crystal or ceramic resonator is used.

Figure 2-5. Overview of Settings When Using Crystal Oscillator on Target System as External Clock



2.3 Power Supply Settings

The power supply is set by JP2 and JP3.

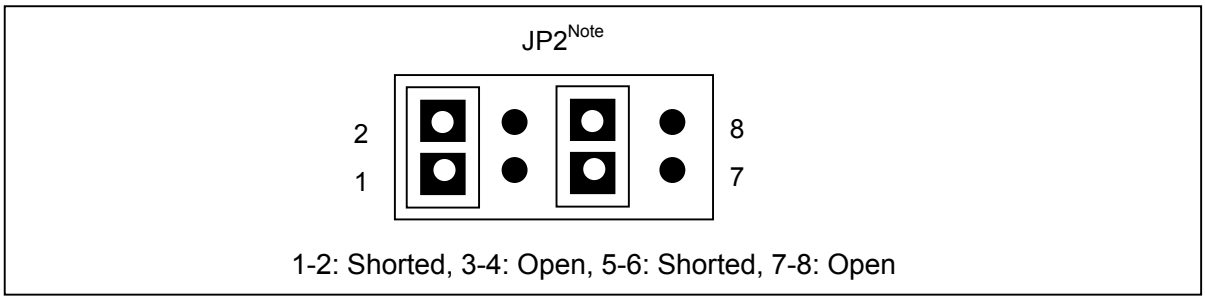
JP2: Setting of V_{DD} and EV_{DD}
JP3: Setting of AV_{DD} and AV_{REF}

2.3.1 JP2 setting (setting of V_{DD} and EV_{DD})

In the IE-703166-MC-EM1, by setting JP2 as shown below, it is possible to automatically select whether to supply V_{DD} and EV_{DD} from inside the emulator, or from the target board by detecting the target board power supply.
(Automatic switching is set by default at shipment).

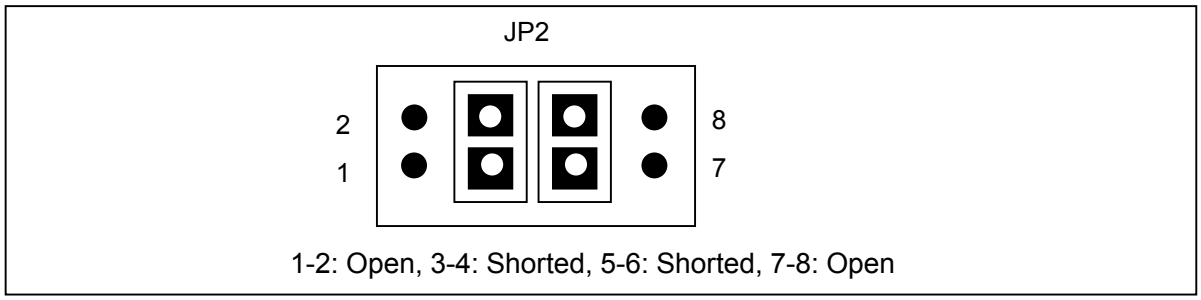
Caution The emulator may be damaged if the JP2 setting is incorrect.

Figure 2-6. JP2 Setting (Automatic Switching)



Note A relay is used for switching the power supply. Depending on the combination of the target system, the relay may repeat switching on/off when the power supply of the target system is turned off and continuously emit a switching sound. In such a case, set the switch as shown in Figure 2-7.

Figure 2-7. JP2 Setting (When Power Supply from Target System Is Used)



V_{DD} and EV_{DD} are always supplied from the target system with the setting shown in Figure 2-7. Note, however, that this setting disables the emulator operation when it is not connected to the target system.

2.3.2 JP3 setting (setting of AV_{DD} and AV_{REF})

The JP3 setting differs when the emulator is operated standalone and when it is operated with the target system.

- When the emulator is operated standalone: See the setting in Figure 2-8
- When the emulator is operated with the target system: See the setting in Figure 2-9

The internal power of the emulator is supplied to AV_{DD} and AV_{REF} when the emulator is operated standalone. AV_{DD} and AV_{REF} are supplied from the target system when the emulator is operated with the target system.

Caution The emulator may be damaged if the JP3 setting is incorrect.

Figure 2-8. JP3 Setting (When Emulator Is Operated Standalone)

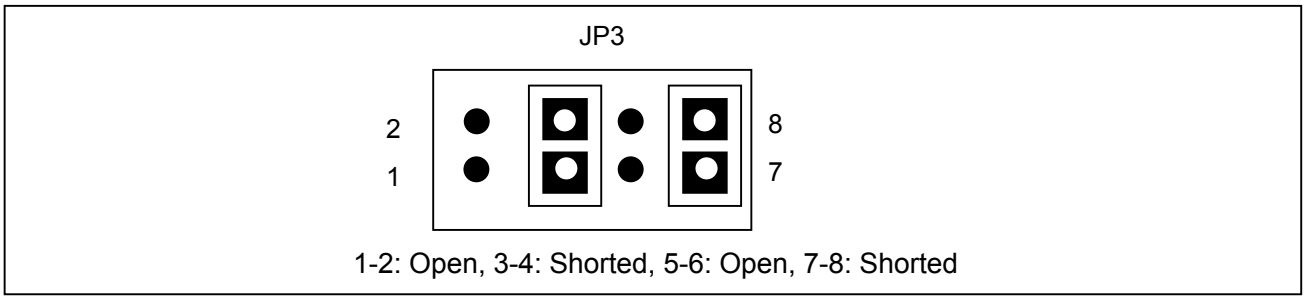
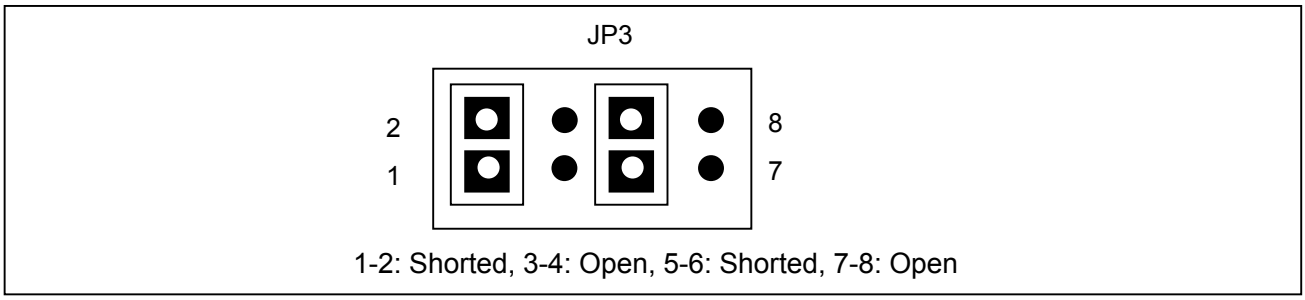


Figure 2-9. JP3 Setting (When Emulator Is Connected to Target System)



Note Settings other than those above are prohibited.

2.4 Emulation Memory

The emulation memory is a 4 MB substitution memory for emulating the memory on the target system or the memory-mapped I/O. It is mounted on the IE-703166-MC-EM1.

2.4.1 Wait settings for emulation memory

A data wait, address wait, and idle state can be set for the emulation memory as shown below.

(1) ID850

The following three alternatives are available on the configuration screen.

	Wait Type	Emulation Memory Access	External Memory Access
WAIT MASK	Data wait	Fixed to 0 waits.	Depends on the DWC0, 1 register settings. WAIT signal is masked.
	Address wait	Fixed to 0 waits.	Depends on the AWC register setting.
	Idle state	Fixed to 0 cycles.	Depends on the BCC register setting.
1 WAIT ACCESS	Data wait	Fixed to 1 wait.	Depends on the DWC0, 1 register settings and WAIT signal status.
	Address wait	Fixed to 0 waits.	Depends on the AWC register setting.
	Idle state	Fixed to 0 cycles.	Depends on the BCC register setting.
TARGET WAIT	Data wait	Depends on the DWC0, 1 register settings. 1 wait when set to 0 waits.	Depends on the DWC0, 1 register settings and WAIT signal status.
	Address wait	Fixed to 0 waits.	Depends on the AWC register setting.
	Idle state	Depends on the BCC register setting.	Depends on the BCC register setting.

(2) Multi

The wait pin can be masked or unmasked by the “Pinmask” command.

	Wait Type	Emulation Memory Access	External Memory Access
WAIT: Mask EMWAIT: Mask	Data wait	Fixed to 0 waits.	Depends on the DWC0, 1 register settings. WAIT signal is masked.
	Address wait	Fixed to 0 waits.	Depends on the AWC register setting.
	Idle state	Fixed to 0 cycles.	Depends on the BCC register setting.
WAIT: Unmask EMWAIT: Mask	Data wait	Fixed to 1 wait.	Depends on the DWC0, 1 register settings and WAIT signal status.
	Address wait	Fixed to 0 waits.	Depends on the AWC register setting.
	Idle state	Fixed to 0 cycles.	Depends on the BCC register setting.
WAIT: Unmask EMWAIT: Unmask	Data wait	Depends on the DWC0, 1 register settings. 1 wait when set to 0 waits.	Depends on the DWC0, 1 register settings and WAIT signal status.
	Address wait	Fixed to 0 waits.	Depends on the AWC register setting.
	Idle state	Depends on the BCC register setting.	Depends on the BCC register setting.

2.4.2 Cautions on emulation memory

(1) The number of waits necessary for accessing emulation memory

The number of waits that need to be inserted for accessing the emulation memory varies depending on the operating frequency of the emulator.

4 MHz ≤ Operating frequency < 25 MHz: 0 waits

25 MHz ≤ Operating frequency ≤ 40.5 MHz: 1 wait

(2) Bus width

Set the bus width to 16 bits (by setting BSn0 of the BSC register to 1). The 8-bit bus cannot be used.

(3) WAIT pin

The number of wait cycles for the emulation memory is not affected by the WAIT pin.

(4) Address wait

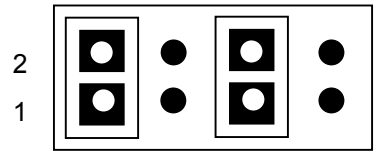
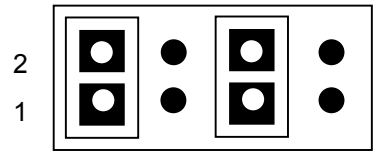
No address waits can be inserted in the emulation memory. Set the waits as shown below if waits must be inserted.

Number of data waits for CS space in the emulation memory	=	Number of address waits for external memory or external I/O	+	Number of data waits for external memory or external I/O

Inserting waits in the emulation memory is effective when you want to equalize the access speeds for the emulation memory and for the external memory or external I/O for performance measurement, etc.

Refer to **2.4.1 Wait settings for emulation memory** for details of how to insert waits in the emulation memory.

CHAPTER 3 FACTORY SETTINGS

Item	Setting	Remark
JP2		The power supply of the target system is automatically detected for operation with this setting. Refer to **2.3 Power Supply Settings** for details.
JP3		The target system is connected for operation with this setting. Change the setting when the emulator is operated standalone. Refer to **2.3 Power Supply Settings** for details.
OSC1	A 40.5 MHz crystal oscillator is mounted.	Refer to **2.2 Clock Settings** for details of the operating frequency setting.

CHAPTER 4 CAUTIONS

This chapter explains the cautions on using the IE-703166-MC-EM1.

4.1 Caution on Clock Generator

The IE-703166-MC-EM1 does not support PLL mode, and always operates in through-clock mode.

When connecting a target system that uses PLL mode and the emulator, directly input the multiplied clock to the emulator. Refer to **2.2 Clock Settings** for details of the clock setting.

When using PLL mode in a microcontroller, the oscillation stabilization time after STOP mode release differs from that of the emulator.

In addition, the CKSEL1 and PLLSEL pins cannot be emulated.

4.2 Caution on Pin Termination

Among the pins connected to the target system, the following pins are left open or pulled up or down inside the emulator.

Pin Name	Pin Handling
RESET	Pulled up with a 33 kΩ resistor.
PLLSEL	Leave open.
CKSEL1	Leave open.
X2	Leave open.
MODE0	Pulled down with a 33 kΩ resistor.
MODE1	Pulled down with a 33 kΩ resistor.

Pin Name	Pin Handling
TRST	Leave open.
TCK	Leave open.
TDI	Leave open.
TMS	Leave open.
TDO	Pulled down with a 33 kΩ resistor.
MODEJ	Leave open.

4.3 Caution on ROM Correction

Although the ROM correction function is not supported, pseudo ROM correction can be emulated using the ID850.

Since this method can be used as a temporary measure, contact an NEC sales representative or distributor for details.

4.4 Caution on WRESF Flag of Watchdog Timer

When a system reset (WDTRES) occurs due to an overflow of the watchdog timer, the RESET signal input from the target system and a CPU reset input from the debugger during WDTRES valid period[Note] are not valid. As a result, the overflow flag (WRESF) of the watchdog timer cannot be cleared.

In such as case, apply the reset again.

Note The WDTRES valid period continues for 120 clocks max. (the number of clocks input to the emulator) if a reset from the target system or a CPU reset from the debugger is not input .

It is 3.0 μs when the input clock is 40.5 MHz.

If a reset is input from the target system or a CPU reset is input from the debugger during the WDTRES valid period, the valid period will be extended by the number of reset input clocks.

CHAPTER 5 REVISION HISTORY

Edition	Revision in This Edition	Page
2nd	Modification of operating frequency in line with change of maximum operating frequency specification from 37.5 MHz to 40.5 MHz	pp. 5, 12, 14, 15, 21, 22, 23