CUSTOMER NOTIFICATION

SUD-DT-03-0480-1-E (1/6)
(Revised from SUD-TT-0013-3-E)
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# IE-703089-MC-EM1
# (Control Code: A, B, C, D, E, F, G, H)

# Operating Precautions

Be sure to read this document before using the product.

# Notes on Using IE-703089-MC-EM1

## 1. Product Version

| Control Code | Board Version | Peripheral Chip | Remark |
|---|---|---|---|
| A | 1.00 | μPD70F3089 (DS1.1) | |
| B | 1.10 | μPD70F3089 (DS1.1) | |
| C | 1.11 | μPD70F3089 (DS1.2) | |
| D | 1.22 | μPD70F3089 (DS2.0 or later) | |
| E | 1.23 | μPD70F3089 (DS2.0 or later) | |
| F | 1.33 | μPD70F3089 (DS2.0 or later) | |
| G | 1.34 | μPD70F3089 (DS2.0 or later) | |
| H | 1.44 | μPD70F3089 (DS2.0 or later) | |

**Employ an IE-703002-MC with a control code of H or later when using this option board.**

## 2. Production History

| No. | Bugs and Changes/Additions to Specifications | Control Code | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A | B | C | D | E | F | G | H |
| 1 | Emulation impossible with target supply voltage below 4.2 V | × | √ | √ | √ | √ | √ | √ | √ |
| 2 | Connection with socket using “YQ-Guide” or with “SWEX-144SD” impossible[Note] | × | √ | √ | √ | √ | √ | √ | √ |
| 3 | Register values related to 3-wire serial I/O channels 5 & 6 cannot be read correctly | × | × | √ | √ | √ | √ | √ | √ |
| 4 | Bug in timer clock selection of timer 6 | × | × | √ | √ | √ | √ | √ | √ |
| 5 | Bug in I/O of port 00 | × | × | × | √ | √ | √ | √ | √ |
| 6 | Bug in accessing the external expansion area | × | × | × | √ | √ | √ | √ | √ |
| 7 | Bug when two FCAN channels are used simultaneously and support for specification change | × | × | × | √ | √ | √ | √ | √ |
| 8 | Addition of device functions<br>(1) IIC bus function<br>(2) Watch timer function | × | × | × | √ | √ | √ | √ | √ |
| 9 | ROM correction function cannot be emulated | Permanent restriction | | | | | | | |
| 10 | Emulation during oscillation stabilization time after RESET release cannot be performed | Permanent restriction | | | | | | | |
| 11 | Restriction on interrupts in STOP/IDLE mode | × | × | × | × | √ | √ | √ | √ |
| 12 | Hi-Z output from the CLKOUT pin cannot be emulated | Permanent restriction | | | | | | | |
| 13 | Bug in external bus interface | × | × | × | × | × | √ | √ | √ |
| 14 | Bug in accessing FCAN area | √ | √ | √ | √ | √ | × | √ | √ |
| 15 | Bug in external bus pin | × | × | × | × | × | × | × | √ |

×: Applicable, √: Not applicable or already corrected

**Note** “YQ-Guide” and “SWEX-144SD” are products of Tokyo Eletech Corporation.

The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, the version can be checked by the label attached to the product.

## 3. Details of Bugs and Added Specifications

No.1 Emulation impossible with target supply voltage below 4.2 V

[Description]

Emulation cannot be performed if the target power supply voltage (Vdd0, Vdd1) is below 4.2 V.

[Workaround]

When the target board is connected, use a power supply voltage (Vdd0, Vdd1) of at least 4.2 V.

This bug has been corrected in control code B or later.

No.2 Connection with socket using “YQ-Guide” or with “SWEX-144SD” impossible

[Description]

A connection cannot be made with a socket using the “YQ-Guide” or with the “SWEX-144SD”.

[Workaround]

When using a socket that uses the “YQ-Guide”, remove the “YQ-Guide” before use.

This bug has been corrected in control code B or later.

No.3 Register values related to 3-wire serial I/O channels 5 & 6 cannot be read correctly

[Description]

I/O register values related to 3-wire serial I/O channels 5 and 6 cannot be read when the CPU clock ($f_{CPU}$) is greater than 10 MHz.

*** This bug only applies to the emulator; it does not occur in the actual CPU.**

[Workaround]

When reading the I/O register values related to 3-wire serial I/O channels 5 and 6 with $f_{CPU}$ operating at more than 10 MHz, set $f_{CPU}$ to 10 MHz or less.

Note that I/O registers can be written as usual when $f_{CPU}$ is operating at more than 10 MHz.

This bug has been corrected in control code C or later.

No.4 Bug in timer clock selection of timer 6

[Description]

If the timer clock selection of timer 6 is set to “TM0 overflow signal” (TCL60 = 07h, TCL61 = 01h), the timer clock will be set to fxx/256, and the TM0 overflow signal will not be able to be selected. (Reading/writing TCL60 = 07h, TCL61 = 01h is possible.)

[Workaround]

There is no workaround.

This bug has been corrected in control code C or later.

No.5 Bug in I/O of port 00

[Description]

Port 00 cannot perform output operations even if set as an output port.

Moreover, port 00 cannot read the correct input value even if set as an input port while the NMI pin function is masked in the debugger. (The operation is performed correctly if port 00 is set as an input port and the NMI pin function is not masked in the debugger.)

[Workaround]

There is no workaround.

This bug has been corrected in control code D or later.

No.6 Bug in accessing the external expansion area

[Description]

The external expansion area (including the FCAN memory area) cannot be read/written.

[Workaround]

There is no workaround.

This bug has been corrected in control code D or later.

No.7 Correction of bug when two FCAN channels are used simultaneously and support for specification change

[Description]

(1) When two FCAN channels are used simultaneously, the received data may be stored in an incorrect message buffer (the last message buffer) or may be discarded.

(2) When two FCAN channels are used simultaneously, incorrect data (the last message buffer) may be transmitted.

(3) The TMR bit of the CANn control register (CnCTRL) was changed.

| TMR | Control Bit for Reception Time Stamp |
|---|---|
| 0 | The value in the time stamp counter is not captured. |
| 1 | The value in the time stamp counter is counted when an EOF is detected on the CAN bus (judged as a valid message). |

* The value in the time stamp counter is not counted even when an SOF is detected on the CAN bus.

[Workaround]

There is no workaround.

This bug has been corrected in control code D or later.

No.8 Addition of device functions

[Description]

(1) IIC bus function

The IICF0 (FFFFF368H) and IICF1 (FFFFF36AH) registers have been added.

(2) Watch timer function

The WTNHC (FFFFF366H) register has been added.

[Workaround]

There is no workaround.

This item has been implemented in control code D or later.

No.9 ROM correction function cannot be emulated

[Description]

The ROM correction function cannot be emulated.

[Workaround]

There is no workaround.

Regard this item as a permanent restriction.

No.10 Emulation during oscillation stabilization time after RESET release cannot be performed

[Description]

Emulation during the oscillation stabilization time after RESET release cannot be performed. Emulation during the oscillation stabilization time after STOP mode release is possible.

[Workaround]

There is no workaround.

Regard this item as a permanent restriction.

No.11 Restriction on interrupts in STOP/IDLE mode

[Description]

The emulator deadlocks if the device is shifted to the STOP/IDLE mode while the interrupt request flag for an interrupt that is not masked is set.

[Workaround 1]

Be sure to clear the non-masked interrupt request flag before shifting to the STOP/IDLE mode. If the device is inadvertently shifted before clearing the flag, execute “Run” → “Stop” or click the  button on the debugger. The program is forcibly terminated. Then, execute “Run” → “CPU Reset” or click the  button.

[Workaround 2]

Do not allow the device to shift to the STOP/IDLE mode while the interrupt request flag for an interrupt that is not masked is set.

This bug has been corrected in control code E or later.

No.12 Hi-Z output from the CLKOUT pin cannot be emulated

[Description]

The Hi-Z output from the CLKOUT pin cannot be emulated. Even if the power save control register (PSC) is set to “Hi-Z output (DCLK1 = 0, DCLK0 = 1)” in the emulator, the same operation as “output enable (DCLK1 = 0, DCLK0 = 0)” is performed.

[Workaround]

There is no workaround.

Regard this item as a permanent restriction.

No.13 Bug in external bus interface

[Description]

When using the external bus interface, the values of read data D0 to D4 may not be read correctly.

[Workaround]

There is no workaround.

This bug has been corrected in control code F or later.

No.14 Bug in accessing FCAN area

[Description]

When an instruction to access the FCAN address area (xxnFF800H to xxnFFFFFH (n = 3, 7, or B)) is allocated to the emulation memory or target memory mapped to the external area and the instruction is executed, the FCAN register may not be able to be read (but it can be written).

[Workaround]

Allocate the instructions to access the FCAN address area to the internal ROM area.

This bug only applies to control code F products.

No.15 Bug in external bus pin

[Description]

The address pin (A[21:16]) does not become Hi-Z in STOP, IDLE, and bus-hold modes.

[Workaround]

There is no workaround.

This bug has been corrected in control code H or later.

## 4. Restriction

The IE-703089-MC-EM1 has the following restriction.

| No. | Restriction |
|---|---|
| 1 | Satisfy the following conditions with other than $V_{DD0}$ = $V_{DD1}$ = $ADCV_{DD}$ = $PORTV_{DD0}$ = $PORTV_{DD1}$ = $PORTV_{DD2}$.<br>(1) $PORTV_{DD1} \leq PORTV_{DD2}$ when using the FCAN controller (restriction of the emulator)<br>(2) $V_{DD0}$ = $ADCV_{DD}$ = 4.5 to 5.5 V when using the A/D converter |