CUSTOMER NOTIFICATION

SUD-DT-03-0123-1-E

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IE-703079-MC-EM1
(Control Code: A, B, C, D, E, F, G, H)

Operating Precautions

Be sure to read this document before using the product.

Notes on Using IE-703079-MC-EM1

1. Product Version

Control Code	Board Version	Peripheral EVA Chip	ROM (IC1)	ROM (IC20)
A	V1.00	UPD70F3079Y DS1.0	HN27C101AG-12 V1.0	CY7C263-20JC V1.0
B	V1.01	UPD70F3079Y DS1.1	HN27C101AG-12 V1.1	CY7C263-20JC V1.0
C	V1.02	UPD70F3079Y ES1.1	HN27C101AG-12 V1.2	CY7C263-20JC V1.0
D	V1.03	UPD70F3079Y ES1.1	HN27C101AG-12 V1.3	CY7C263-20JC V1.0
E	V1.04	UPD70F3079Y DS2.0	HN27C101AG-12 V1.3	CY7C263-20JC V1.0
F	V1.24	UPD70F3079AY DS1.1	HN27C101AG-12 V1.3	CY7C263-20JC V1.0
G	V1.34	UPD70F3079AY DS1.1	HN27C101AG-12 V1.3	CY7C263-20JC V1.0
H	V1.44	UPD70F3079AY DS1.1	HN27C101AG-12 V1.3	CY7C263-20JC V1.0

Employ an IE-703002-MC with a control code of H or later when using this option board.

2. Product History

No.	Bugs and Changes/Additions to Specifications	Control Code [Note]							
		A	B	C	D	E	F	G	H
1	P0.0 cannot be used.	×	√	√	√	√	√	√	√
2	POC function cannot be used.	Permanent restriction							
3	When FCAN memory is accessed, bus cycle is output from the external expansion pin.	Permanent restriction							
4	Restriction on P4, 5, 6, 9, and 11 in input mode	×	√	√	√	√	√	√	√
5	Restriction when P11 is set as an alternate function pin	×	×	√	√	√	√	√	√
6	The high-level signal output from P0.0 is lower than the PortV_{DD} potential by about 1 V.	×	×	×	√	√	√	√	√
7	The high-level signal output from P0.0 is fixed at 5 V.	Permanent restriction							
8	Restriction on the FCAN function when the WAIT pin is used	×	×	×	√	√	√	√	√
9	Caution when FCAN memory is accessed	×	×	×	×	√	√	√	√
10	Restriction on external clock	Permanent restriction							
11	ROM correction function cannot be emulated	Permanent restriction							
12	Emulation during oscillation stabilization time after RESET release cannot be performed	Permanent restriction							
13	Restriction on interrupts in STOP/IDLE mode	×	×	×	×	×	×	√	√
14	Modification of emulation target CPU	×	×	×	×	×	√	√	√
15	Hi-Z output from the CLKOUT pin cannot be emulated	Permanent restriction							
16	Bug in external bus interface	×	×	×	×	×	×	×	√

×: Applicable, √: Not applicable or already corrected

Note The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

3. Details of Bugs and Added Specifications

No.1 P0.0 cannot be used

[Description]

P0.0 cannot be used.

[Workaround]

There is no workaround.

This bug has been corrected in control code B.

No.2 POC function cannot be used

[Description]

POC function cannot be used.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.3 When FCAN memory is accessed, bus cycle is output from the external expansion pin

[Description]

When FCAN memory is accessed, bus cycle is output from the external expansion pin.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.4 Restriction on P4, 5, 6, 9, and 11 in input mode

[Description]

If P4, 5, 6, 9, and 11 are in input mode, the potential of the pins is lowered even if a pull-up resistor is connected on the target system (approx. 2.5 to 4 V).

[Workaround]

There is no workaround.

This bug has been corrected in control code B.

No.5 Restriction when P11 is set as an alternate function pin

[Description]

If PM11 is set to output mode while P11 is set as a multiplexed pin (CAN control pin), the potential of the low-level output signal is not lowered to less than 2.5 V.

[Workaround]

There is no workaround.

This bug has been corrected in control code C.

No.6 The high-level signal output from P0.0 is lower than the PortVDD potential by about 1 V.

[Description]

The high-level signal output from P0.0 is lower than the PortVDD potential by about 1 V.

[Workaround]

There is no workaround.

This bug has been corrected in control code D.

No.7 The high-level signal output from P0.0 is fixed at 5 V.

[Description]

The high-level output from P0.0 is fixed at 5 V regardless of PortVDD.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.8 Restriction on the FCAN function when the WAIT pin is used

[Description]

The FCAN function cannot be used if the WAC flag of the PAC register is set to the WAIT pin.

[Workaround]

There is no workaround.

This bug has been corrected in the control code D model.

No.9 Caution when FCAN memory is accessed

[Description]

The in-circuit emulator deadlocks if addresses between 0xnffe00 and 0xnfffff (n = 3, 7, b) of the FCAN address area are accessed (this area is unusable).

[Workaround]

Do not access addresses between 0xnffe00 and 0xnfffff (n = 3, 7, b).

This bug has been corrected in control code E.

No.10 Restriction on external clock

[Description]

Emulation cannot be performed externally with the main clock or the subclock.

[Workaround]

Use the clock in the emulator.

This will be designated as a permanent restriction.

No.11 ROM correction function cannot be emulated

[Description]

The ROM correction function cannot be emulated.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.12 Emulation during oscillation stabilization time after RESET release cannot be performed

[Description]

Emulation during the oscillation stabilization time after RESET release cannot be performed.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.13 Restriction on interrupts in STOP/IDLE mode

[Description]

The emulator deadlocks if the device is shifted to the STOP/IDLE mode while the interrupt request flag for an interrupt that is not masked is set.

[Workaround 1]

Be sure to clear the non-masked interrupt request flag before shifting to the STOP/IDLE mode. If the device is inadvertently shifted before clearing the flag, execute "Run" → "Stop" or click the  button on the debugger. The program is forcibly terminated. Then, execute "Run" → "CPU Reset" or click the  button.

[Workaround 2]

Do not allow the device to shift to the STOP/IDLE mode while the interrupt request flag for an interrupt that is not masked is set.

This bug has been corrected in control code G.

No.14 Modification of emulation target CPU

[Description]

The emulation target CPUs have been changed from the μPD70F3079Y, 70307xY (non-A versions) to the μPD70F3079AY, 70307xAY (A versions).

* Care must be taken because the initial value of the oscillation stabilization time selection register (OSTS) differs between the μPD70F3079Y, 70307xY (non-A products) and the μPD70F3079AY, 70307xAY (A products).

* The Hi-Z output from the CLKOUT pin cannot be emulated.

[Workaround]

There is no workaround.

This change has been implemented in control code F.

No.15 Hi-Z output from the CLKOUT pin cannot be emulated

[Description]

The Hi-Z output from the CLKOUT pin cannot be emulated. Even if the power save control register (PSC) is set to "Hi-Z output (DCLK1 = 0, DCLK0 = 1)" in the emulator, the same operation as "output enable (DCLK1 = 0, DCLK0 = 0)" is performed.

[Workaround]

There is no workaround.

This will be designated as a permanent restriction.

No.16 Bug in external bus interface

[Description]

The data cannot be read correctly when using the external bus interface.

[Workaround]

There is no workaround.

This bug has been corrected in control code H.

4. Cautions

When using the FCAN function, implement the following procedure on startup of the debugger.

a) Before startup of the debugger, supply power to pin VDD0 (GC package: pin 8, GF package: pin 11) on the target board

b) Set the memory mapping on the debugger as shown below.

Attribute: Target memory

Mapping address: nFF800H to nFFFFFH (n = 3, 7, B)

c) Do not mask WAIT and HLDRQ when accessing the FCAN memory.