CUSTOMER NOTIFICATION

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IE-703079-MC-EM1
(Control Code: A, B, C, D, E)

RESTRICTIONS

Be sure to read this document before using the product.

1. PRODUCT VERSION

Product name: IE-703079-MC-EM1

Control code	Board version	Peripheral evaluation chip	FPGA	ROM
A	V1.00	UPD70F3079Y DS1.0	HN27C101AG-12 V1.0	CY7C263-20JC V1.0
B	V1.01	UPD70F3079Y DS1.1	HN27C101AG-12 V1.1	CY7C263-20JC V1.0
C	V1.02	UPD70F3079Y ES1.1	HN27C101AG-12 V1.2	CY7C263-20JC V1.0
D	V1.03	UPD70F3079Y ES1.1	HN27C101AG-12 V1.3	CY7C263-20JC V1.0
E	V1.04	UPD70F3079Y DS2.0	HN27C101AG-12 V1.3	CY7C263-20JC V1.0

Note The control code is indicated by the second character from the left in the 10 character manufacturing code beginning with E.

Employ an IE-703002-MC with a control code of H or later when using this option board.

2. OVERVIEW OF RESTRICTIONS

No.	Restrictions	Control code				
		A	B	C	D	E
1	P0.0 cannot be used.	×	√	√	√	√
2	POC function cannot be used.	Permanent restriction				
3	When FCAN memory is accessed, bus cycle is output from the external expansion pin.	Permanent restriction				
4	Restriction on P4, 5, 6, 9, and 11 in input mode	×	√	√	√	√
5	Restriction when P11 is set as a multiplexed pin	×	×	√	√	√
6	The high-level signal output from P0.0 is lower than the Port V_{DD} potential by about 1 V.	×	×	×	√	√
7	The high-level signal output from P0.0 is fixed at 5 V.	Permanent restriction				
8	Restriction on the FCAN function when the WAIT pin is used	×	×	×	√	√
9	Caution when FCAN memory is accessed	×	×	×	×	√
10	Restrictions on external clock	Permanent restriction				

√: Already solved

×: Corresponding restriction exists

3. DETAILS OF RESTRICTIONS

(1) P0.0 cannot be used

Description: P0.0 cannot be used.

Workaround: There is no workaround. This bug has been corrected in the control code B model.

(2) POC function cannot be used

Description: POC function cannot be used.

Workaround: There is no workaround. This will be designated as a permanent restriction.

(3) When FCAN memory is accessed, bus cycle is output from the external expansion pin

Description: When FCAN memory is accessed, bus cycle is output from the external expansion pin.

Workaround: There is no workaround. This will be designated as a permanent restriction.

(4) Restriction on P4, 5, 6, 9, and 11 in input mode

Description: If P4, 5, 6, 9, and 11 are in input mode, the potential of the pins is lowered even if a pull-up resistor is connected on the target system (approx. 2.5 to 4 V).

Workaround: There is no workaround. This bug has been corrected in the control code B model.

(5) Restriction when P11 is set as a multiplexed pin

Description: If PM11 is set to output mode while P11 is set as a multiplexed pin (CAN control pin), the potential of the low-level output signal is not lowered to less than 2.5 V.

Workaround: There is no workaround. This bug has been corrected in the control code C model.

(6) The high-level signal output from P0.0 is lower than the Port V_{DD} potential by about 1 V.

Description: The high-level signal output from P0.0 is lower than the Port V_{DD} potential by about 1 V.

Workaround: There is no workaround. This bug has been corrected in the control code D model.

(7) The high-level signal output from P0.0 is fixed at 5 V.

Description: The high-level output from P0.0 is fixed at 5 V regardless of Port V_{DD}.

Workaround: There is no workaround. This will be designated as a permanent restriction.

(8) Restriction on the FCAN function when the WAIT pin is used

Description: The FCAN function cannot be used if the WAC flag of the PAC register is set to the WAIT pin.

Workaround: There is no workaround. This bug has been corrected in the control code D model.

(9) Caution when FCAN memory is accessed

Description: The in-circuit emulator deadlocks if addresses between 0xnffe00 and 0xnffffff (n = 3, 7, b) of the FCAN address area are accessed (this area is unusable).

Workaround: Do not access addresses between 0xnffe00 and 0xnffffff (n = 3, 7, b). This bug has been corrected in the control code E model.

(10) Restrictions on external clock

Description: Emulation cannot be performed externally with the main clock or the subclock.

Workaround: Use the clock in the emulator. This will be designated as a permanent restriction.

4. CAUTIONS

When using the FCAN function, implement the following procedure on startup of the debugger.

a) Before startup of the debugger, supply power to pin VDD0 (GC package: pin 8, GF package: pin 11) on the target board

b) Set the memory mapping on the debugger as shown below.
Attribute: Target memory
Mapping address: nFF800H to nFFFFFH (n = 3, 7, 8)

c) Do not mask WAIT and HLDRQ when accessing the FCAN memory.