With I²C bus interface (RIIC), one clock cycle may be inserted between the ninth clock cycle of master reception and stop condition issuance.

When this clock affects the communication, follow the avoidance flow indicated below.

1. Conditions
   (1) RX610, 62N, 621, 62T groups
      - When data is read from ICDRR after the falling edge of the ninth clock of master reception and writing SP=1 are detected at the same time in the RIIC.
      - After SP=1 is written, when the falling edge of the ninth clock cycle of master reception and data reading from ICDRR are detected at the same time in the RIIC.

   (2) RX630, 63N, 631 groups
      - While holding at low at the falling edge of the ninth clock cycle, writing SP=1 and reading data from ICDRR are performed in a row.
      - When data is read from ICDRR after the falling edge of the ninth clock of master reception and writing SP=1 are detected at the same time in the RIIC.
      - After SP=1 is written, when the falling edge of the ninth clock cycle of master reception and data reading from ICDRR are detected at the same time in the RIIC.

2. Phenomenon
   One clock cycle is inserted between the ninth clock cycle of master reception and stop condition issuance.
3. Avoidance Flow

One clock cycle is prevented from inserting before issuing stop condition by writing to the ICMR3.RDRFS bit and the ICMR3.ACKBT bit again when receiving master. Add the procedures marked in red indicated below to the flowchart in the user’s manual.

“xx” as in Figure xx.10 indicates the chapter of I2C of the user’s manual respectively. Please refer to the “Target products and Reference” for details.

Figure xx.10 Example of Master Reception Flowchart (7-Bit Address Format)
### Target products and Reference

<table>
<thead>
<tr>
<th>Group</th>
<th>Title</th>
<th>Rev.</th>
<th>Document No.</th>
<th>Chapter of i²C</th>
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<tbody>
<tr>
<td>RX610 group</td>
<td>RX610 group User’s Manual, Hardware section</td>
<td>Rev.1.10</td>
<td>R01UH0032EJ0110</td>
<td>22</td>
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<td>R01UH0041EJ0090</td>
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