While timeout detection function of \( \text{I}^2\text{C} \) bus interface (RIIC) is set to CMR1.CKS [2:0] ≠ 000, timeout is detected even when communications are proceeding correctly. To avoid this, use registered disclosed in this document and follow the avoidance flow. In this avoidance flow, every time data is accessed, write 0000h to the timeout internal counter and clear counter. Thus, it is applicable only to data transfer using CPU or one using DTC. When you use DMAC for data transfer of RIIC, you need to set ICMR1.CKS [2:0] = 000b or change it to transfer using CPU or one using DTC.

1. Condition
   When using timeout detection function of \( \text{I}^2\text{C} \) bus interface (RIIC) under setting of CMR1.CKS [2:0] ≠ 000.

2. Phenomenon
   Even when communications are proceeding correctly, timeout is detected from a set of ICFER.TMOE bit after a certain period of time for detection has elapsed.

3. Disclosed register
   - (1) ICMR2.TMWE bit (b3) of \( \text{I}^2\text{C} \) bus mode register (ICMR2) will be disclosed.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>b3</td>
<td>TMWE</td>
<td>Timeout internal counter write enable bit</td>
<td>0: Writing to internal counter of timeout detection function is disabled 1: Writing to internal counter of timeout detection function is enabled When this bit is set to “1”, the address of timeout internal counter (TMOCNT_L/U) is allocated to the address of SARL0/SARU0.</td>
</tr>
</tbody>
</table>
(2) Disclose the timeout internal counter register (TMOCNT).

Timeout internal counter (TMOCNT)

Address
RIIC0.TMOCNT_L 0008 830Ah*, RIIC1.TMOCNT_L 0008 832Ah*,
RIIC0.TMOCNT_U 0008 830Bh*, RIIC1.TMOCNT_U 0008 832Bh*

*Same addresses with ones of the slave address registers, SARL0, SARU0. Care should be taken.

- TMOS=0 (Long mode)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Symbol</th>
<th>Bit name</th>
<th>Description</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>b15-8</td>
<td>TMOCNT_U</td>
<td>Timeout internal counter</td>
<td>Timeout internal counter high-order*1</td>
<td>W*2</td>
</tr>
<tr>
<td>b7-0</td>
<td>TMOCNT_L</td>
<td>Timeout internal counter</td>
<td>Timeout internal counter low-order</td>
<td></td>
</tr>
</tbody>
</table>

*1: With TMOS=1 (Short mode), b15-b12 are reserved bits. They are writable, however value written is disabled.

*2: Value in timeout internal counter cannot be read. When value is read, the read value is FFFFh.

Timeout internal counter (TMOCNT_L/TMOCNT_U) is initialized (0000h) after a reset, while ICCR1.IICRST=1 or ICFER.TMOE=1 and PCLK/1 is selected with ICMR1.CKS[2:0]=000b setting, and when counter clear conditions specified by TMOH/TMOL of ICMR2 (SCL rising edge/falling edge detection) are satisfied.
4. Avoidance Flow

To avoid this, add the procedures marked in red indicated below to the flowchart in the user’s manual.

“xx” as in Figure xx.5 indicates the chapter of I2C of the user’s manual respectively. Please refer to the “Target products and Reference” for details.

Figure xx.5  Example of RIIC Initialization Flow

<table>
<thead>
<tr>
<th>n=0 to 2</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCR1.ICE=1</td>
<td>RIIC transfer operation enabled</td>
</tr>
<tr>
<td>ICMR2.TMWE=1</td>
<td>RIIC transfer operation enabled</td>
</tr>
<tr>
<td>TMOCNT=0000h</td>
<td>RIIC transfer operation enabled</td>
</tr>
<tr>
<td>ICFER.TMOE=1</td>
<td>RIIC transfer operation enabled</td>
</tr>
<tr>
<td>Set ICFER</td>
<td>These procedures need to be added only when using timeout function. Not needed when not using timeout function</td>
</tr>
<tr>
<td>Set ICER</td>
<td>These procedures need to be added only when using timeout function. Not needed when not using timeout function</td>
</tr>
<tr>
<td>ICCR1.IICRST=0</td>
<td>Cancel RIIC internal reset</td>
</tr>
<tr>
<td>Set SARLn and SARUn. Set ICSER.</td>
<td>Set slave address format and slave address</td>
</tr>
<tr>
<td>Set CKS[2:0] in ICMR1 and ICBRL/ICBRH</td>
<td>Set transfer bit rate*1</td>
</tr>
<tr>
<td>Set ICMR2 and ICMR3</td>
<td>RIIC function disabled</td>
</tr>
<tr>
<td>ICCR1.ICE=0</td>
<td>RIIC internal reset</td>
</tr>
<tr>
<td>ICCR1.IICRST=1</td>
<td>RIIC internal reset</td>
</tr>
</tbody>
</table>

*1: When the RIIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.

*2: Set these registers as necessary.
**Figure xx.6** Example of Master Transmission Flowchart

---

1. **Initial settings**
   - ICCR2.BBSY=0?
     - Yes
     - ICCR2.ST=1
   - ICSR2.NACKF=0?
     - Yes
     - ICSR2.TDRE=1?
       - Yes
       - TMOCNT=0000h
     - No
   - All data transmitted?
     - Yes
     - ICSR2.TEND=1?
       - Yes
       - TMOCNT=0000h
       - ICSR2.STOP=0
       - ICCR2.SP=1
     - No
     - ICSR2.STOP=0
   - No
   - ICSR2.TSTOP=1?
     - Yes
     - TMOCNT=0000h
     - ICSR2.NACKF=0
     - ICSR2.STOP=0
   - End of master transmission

---

2. **Check I2C bus occupation and issue a start condition.**

3. **Transmit slave address and W (first byte).**

4. **Check ACK and set transmit data.**

5. **Check end of last data transmission and issue a stop condition.**

6. **Check stop condition issuance.**

7. **Processing for the next transfer operation.**

---

*These procedures need to be added only when using timeout function. Not needed when not using timeout function.*
Figure xx.10  Example of Master Reception Flowchart (7-Bit Address Format)

[Diagram showing the flowchart with steps numbered 1 to 9, indicating the process of master reception with conditions and actions listed accordingly.]

*1) These procedures need to be added only when using timeout function. Not needed when not using timeout function.
**Figure xx.14 Example of Slave Transmission Flowchart**

1. **Initial settings**
   - ICSR2.NACKF=0?
     - Yes
       - TMOCNT=0000h
     - No

2. Write data to ICDRT
   - Yes
   - No

3. All data transmitted?
   - Yes
   - No

4. ICSR2.TEND=1?
   - Yes
   - No

5. **End of slave transmission**

*1: These procedures need to be added only when using timeout function. Not needed when not using timeout function.

**Figure xx.17 Example of Slave Reception Flowchart**

1. **Initial settings**

2. ICSR2.STOP=0?
   - Yes
   - No

3. ICSR2.RDRF=1?
   - Yes
   - No

4. Read ICDRR
   - Yes
   - No

5. All data received?
   - Yes
   - No

6. ICSR2.STOP=1?
   - Yes
   - No

7. Read ICDRR (last data)
   - Yes
   - No

8. **End of slave reception**

*1: These procedures need to be added only when using timeout detection function. Not needed when not using timeout detection function.
5. Avoidance when using DTC

When writing transmit data to ICDRT or reading receive data from ICDRR by the DTC during master transmission/reception, use the following flow to avoid the phenomenon. Set the DTC to chain transfer, and clear internal counter every time transmit data or receive data is transferred.

Master reception flowchart is indicated below.
This flowchart shows only flow involved with DTC transfer. For the rest of the flow, refer to the flowcharts indicated on page 3 to 6.

(1) Initial settings flow: What is indicated on page 3 + DTC setting
The DTC needs to be set to enable the following operation.
Set the DTC to chain transfer.
・First chain transfer (Chain transfer 1): Write 0000h to TMOCNT
・Subsequent chain transfer (Chain transfer 2): Transfer specified by user (Read ICDRR, etc)

(2) Example of flowchart during N-2 times transfer by DTC (excerpt comments from the flowchart on page 5)
### Target Products and Reference

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