Date: Mar. 10, 2020

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A0052A/E	Rev.	1.00
Title	How to access data flash without using device driver		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S124 MCU Group Renesas Synergy™ S128 MCU Group Renesas Synergy™ S1JA MCU Group Renesas Synergy™ S3A1 MCU Group Renesas Synergy™ S3A3 MCU Group Renesas Synergy™ S3A6 MCU Group Renesas Synergy™ S3A7 MCU Group	Lot No. All	Reference Document	S124 Microcontroller Group User's Manual Rev.1.20 S128 Microcontroller Group User's Manual Rev.1.10 S1JA Microcontroller Group User's Manual Rev.1.40 S3A1 Microcontroller Group User's Manual Rev.1.20 S3A3 Microcontroller Group User's Manual Rev.1.10 S3A6 Microcontroller Group User's Manual Rev.1.20 S3A7 Microcontroller Group User's Manual Rev.1.40		

It is necessary that DFLCTL.DFLEN bit is set to 1 before accessing the data flash.

To access the memory, perform the following procedure:

(1) Write 1 to bit 0 (DFLEN) of the data flash control register (DFLCTL).

(2) Wait for the setup to finish for software timer, etc.

The time setup takes differs for each operating mode.

<Setup time for each operating mode>

- HS (High-speed) mode: 5 us
- LS (Low-speed) mode: 720 ns
- LP (Low-power) mode: 720 ns
- LV (Low-voltage) mode: 10 us

(3) After the wait, the data flash memory can be accessed.

Data flash Control Register (DFLCTL)

Address(es) 407E_C090h

	b7	b6	b5	b4	b3	b2	b1	b0
								DFLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DFLEN	data flash Access Enable	0: Access to the data flash is disabled 1: Access to the data flash is enabled	R/W
b7-b1	-	Reserved	Read data is 0. The write value should be 0.	R/W

The DFLCTL register is to enable or disable accessing (reading, programming, and erasing) of the data flash. After setting the DFLCTL.DFLEN bit, Data Flash STOP recovery time (tDSTOP) is nccessary before reading the data flash or entering the data flash P/E mode.