To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A304A/E	Rev.	1.0
Title	H8SX/1582 Hardware Manual: Amendment to the List of Registers		Information Category	Technical Notification		
Applicable Product	H8SX/1582	Lot No. All lots	Reference Document	H8SX/1582 Hardware Manual (REJ09B0199-0100Z Rev.1.00)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the amendment to the list of registers in the H8SX/1582 Hardware Manual, Rev.1.00 (REJ09B0199-0100Z).

1. Addition to Section 20.1, Register Addresses (Address Order)
The following registers are added; port B data direction register (PBDDR), port B input buffer control register (PBICR), port I data direction register (PIDDR), port I input buffer control register (PIICR), and port I pull-up MOS control register.

(1) Port B data direction register (PBDDR) on page 637

[Before change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port A data direction register	PADDR	8	H'FFB89	I/O port	8	2Pϕ/2Pϕ
Port D data direction register	PDDDR	8	H'FFB8C	I/O port	8	2Pϕ/2Pϕ

[After change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port A data direction register	PADDR	8	H'FFB89	I/O port	8	2Pϕ/2Pϕ
Port B data direction register	PBDDR	8	H'FFB8A	I/O port	8	2Pϕ/2Pϕ
Port D data direction register	PDDDR	8	H'FFB8C	I/O port	8	2Pϕ/2Pϕ

(2) Port B input buffer control register (PBICR) on page 638

[Before change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port A input buffer control register	PAICR	8	H'FFB99	I/O port	8	2Pϕ/2Pϕ
Port D input buffer control register	PDICR	8	H'FFB9C	I/O port	8	2Pϕ/2Pϕ

[After change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port A input buffer control register	PAICR	8	H'FFB99	I/O port	8	2Pϕ/2Pϕ
Port B input buffer control register	PBICR	8	H'FFB9A	I/O port	8	2Pϕ/2Pϕ
Port D input buffer control register	PDICR	8	H'FFB9C	I/O port	8	2Pϕ/2Pϕ

(3) Port I data direction register (PIDDR) on page 638

[Before change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port H data direction register	PHDDR	8	H'FFBA8	I/O port	8	2Pϕ/2Pϕ
Port J data direction register	PJDDR	8	H'FFBAA	I/O port	8	2Pϕ/2Pϕ

[After change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port H data direction register	PHDDR	8	H'FFBA8	I/O port	8	2Pϕ/2Pϕ
Port I data direction register	PIDDR	8	H'FFBA9	I/O port	8	2Pϕ/2Pϕ
Port J data direction register	PJDDR	8	H'FFBAA	I/O port	8	2Pϕ/2Pϕ

(4) Port I input buffer control register (PIICR) on page 638

[Before change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port H input buffer control register	PHICR	8	H'FFBAC	I/O port	8	2Pϕ/2Pϕ
Port J input buffer control register	PJICR	8	H'FFBAE	I/O port	8	2Pϕ/2Pϕ

[After change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port H input buffer control register	PHICR	8	H'FFBAC	I/O port	8	2Pϕ/2Pϕ
Port I input buffer control register	PIICR	8	H'FFBAD	I/O port	8	2Pϕ/2Pϕ
Port J input buffer control register	PJICR	8	H'FFBAE	I/O port	8	2Pϕ/2Pϕ

(5) Port I pull-up MOS control register (PIPCR) on page 638

[Before change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port H pull-up MOS control register	PHPCR	8	H'FFBB8	I/O port	8	2Pϕ/2Pϕ
Port J pull-up MOS control register	PJPCR	8	H'FFBBA	I/O port	8	2Pϕ/2Pϕ

[After change]

Register Name	Abbr.	Number of Bits	Address*	Module	Data Width	Access Cycles (Read/Write)
Port H pull-up MOS control register	PHPCR	8	H'FFBB8	I/O port	8	2Pϕ/2Pϕ
Port I pull-up MOS control register	PIPCR	8	H'FFBB9	I/O port	8	2Pϕ/2Pϕ
Port J pull-up MOS control register	PJPCR	8	H'FFBBA	I/O port	8	2Pϕ/2Pϕ

2. Addition to Section 20.2, Register Bits

(1) PORTI on page 651

[Before change]

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
PORTH	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	I/O port
PORTJ	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	

[After change]

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
PORTH	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	I/O port
PORTI	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	
PORTJ	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	