To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A357A/E	Rev.	1.00
Title	H8SX: Problems in data transfer by SCI		Information Category	Technical Notification		
Applicable Product	H8SX/1650 Group H8SX/1651 Group H8SX/1657 Group	Lot No. All lots	Reference Document	H8SX/1650 Group Hardware Manual (REJ09B0311-0100, Rev. 1.0) H8SX/1651 Group Hardware Manual (REJ09B0248-0100, Rev. 1.0) H8SX/1657 Group Hardware Manual (REJ09B0341-0100, Rev. 1.0)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of the problems in data transfer by the SCI that occur when writing to a specific register of the H8SX/1650, H8SX/1651, and H8SX/1657 Groups of microcontrollers. Please take this information into consideration when using these products.

[Applicable Products]

H8SX/1650 Group, H8SX/1651 Group, and H8SX/1657 Group

[Applicable Module]

Serial communication interface (SCI)

[Applicable Registers]

Serial control register (SCR): Controls transmission/reception and interrupts and selects a clock source.

Smart card control register (SCMR): Selects the communication format and a clock source for the on-chip baud rate generator.

Serial mode register (SMR): Selects smart card interface mode and its format.

[Phenomena]

The following phenomena (A) to (C) can occur during execution of writing to any of the applicable registers of the channel on which data transmission or reception is in progress.

(A) If writing to an applicable register is executed for a channel that is transmitting data, the bits being transmitted during writing are illegally inverted.

(B) If writing to an applicable register is executed for a channel that is receiving data, the bits being received during writing are illegally inverted.

(C) If writing to an applicable register is executed immediately after clearing of the overrun error flag, the first SCK clock pulse is not output normally (improper duty cycle), which prevents correct reception.

[Operating Conditions, Operations Causing the Problem, and Phenomena]

Operating Condition			Operation Causing the Problem		Phenomena	Category
Communication Mode	Clock Source	Transmission /Reception	Applicable Register	Operation		
Synchronous	Internal clock (SCK output)	Transmission	SCR	Writing to the applicable register of the channel that is transmitting data	The bits being transmitted during writing are illegally inverted.	(A)
		Reception	SCR SCMR*2	Writing to the applicable register of the channel that is receiving data	The bits being received during writing are illegally inverted.	(B)
			SCR	Writing to the applicable register immediately after clearing of the overrun error flag	The SCK clock output becomes abnormal and reception cannot be performed correctly.	(C)
	External clock input	Transmission	SCMR*2	Writing to the applicable register of the channel that is transmitting data	The bits being transmitted during writing are illegally inverted.	(A)
		Reception		Writing to the applicable register of the channel that is receiving data.	The bits being received during writing are illegally inverted.	(B)
Asynchronous	Internal clock *1	Reception	SCR SCMR*2	Writing to the applicable register of the channel that is receiving data	The bits being received during writing are illegally inverted.	(B)
	External clock input	Transmission	SMR*2	Writing to the applicable register of the channel that is transmitting data	The bits being transmitted during writing are illegally inverted.	(A)
Smart card interface	Internal clock	Reception	SCR	Writing to the applicable register of the channel that is receiving data	The bits being received during writing are illegally inverted.	(B)

Notes: 1. There are exceptional cases under the operating conditions of “asynchronous mode/internal clock/reception.” The data transfer error does not occur when there is sufficient margin in data reception or when the transfer rate of the transmitting device is slower than that of the H8SX.

2. The following precautionary description is given in the hardware manual:
”Initialize the SCI as described in the sample flowchart. When the operating mode, transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change.”

[Provisionary Countermeasure]

Use the following procedure to make sure if your usage fall under the category that causes the problem.

(1) Operating condition
Check if your usage fits into any of the combinations of communication mode (synchronous/asynchronous/smart card interface), clock source selection (internal/external clock), and whether transmission or reception shown in the table above.

(2) Writing to the applicable register and its timing
If your usage fits into the operating conditions above, check to see if writing is performed with the timing shown above.

If your usage is found to be the case through steps (1) and (2), the following countermeasure must be taken to avoid the problem.

Cases (A) and (B): Do not write to the applicable registers during data transmission or reception.

Case (C): Clear the overrun error flag after writing to the SCR register.

For the case of “asynchronous/internal clock (*1)”, no countermeasure in software is needed as long as there is sufficient margin in reception. Check to see if there is a 20 to 30% margin, as is written in the hardware manual under the section titled “Receive Data Sampling Timing and Reception Margin in Asynchronous Mode.”

[Permanent Countermeasure]

Renesas will modify the circuitry of the applicable H8SX products and release the revised versions until September 2007.