To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A375A/E	Rev.	1.00
Title	H8S/2649: Amendment for Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8S/2649 Group	Lot No. All Lots	Reference Document	H8S/2649 Group Hardware Manual (REJ09B0200-0200)		

We would like to inform you about the amendment for the H8S/2649 Group Hardware Manual

1. Overview

【Before】 General I/O ports I/O pins: 97

【After】 General I/O ports I/O pins: 92

2. Data Transfer Controller Table8.1

【Before】

Interrupt Source	VectorNumber	DTC Vector Address
RXI_1	85	H'04A8
TXI_1	86	H'04AA

【After】

Interrupt Source	VectorNumber	DTC Vector Address
RXI_1	85	H'04AA
TXI_1	86	H'04AC

3. Watchdog Timer

Timer Control/Status Register (TCSR) TCSR_1 bit2 to bit0

【Before】

When PSS = 1 (values in parentheses are for ϕSUB =32.768 kHz):

000: ϕSUB/2 (cycle: 13.1 ms)

001: ϕSUB/4 (cycle: 26.2 ms)

010: ϕSUB/8 (cycle: 52.4 ms)

011: ϕSUB/16 (cycle: 104.9 ms)

100: ϕSUB/32 (cycle: 209.7 ms)

101: ϕSUB/64 (cycle: 419.4 ms)

110: ϕSUB/128 (cycle: 838.9 ms)

111: ϕSUB/256 (cycle: 1.6777 s)

【After】

When PSS = 1 (values in parentheses are for ϕSUB =32.768 kHz):

000: ϕSUB/2 (cycle: 15.6 ms)

001: ϕSUB/4 (cycle: 31.3 ms)

010: ϕSUB/8 (cycle: 62.5 ms)

011: ϕSUB/16 (cycle: 125 ms)

100: ϕSUB/32 (cycle: 250 ms)

101: ϕSUB/64 (cycle: 500 ms)

110: ϕSUB/128 (cycle: 1 s)

111: ϕSUB/256 (cycle: 2 s)

4. Serial communication Interface

Table 13.3 to Tabel 13.9 BRR Settings for Various Bit Rates

【Before】 24MHz : Yes

【After】 24MHz: No

Table 13.12

【Before】 Channel1,4 :Nothing

【After】

Channel	Name	Interrupt Source	Interrupt Flag	DTC Activation
1	ERI_1	Receive Error	ORER,FER,PER	Not possible
	RXI_1	Receive Data Full	RDRF	Possible
	TXI_1	Transmit Data Empty	TDRE	Possible
	TEI_1	Transmission End	TEND	Not possible
4	ERI 4	Receive Error	ORER,FER,PER	Not possible
	RXI_4	Receive Data Full	RDRF	Possible
	TXI_4	Transmit Data Empty	TDRE	Possible
	TEI_4	Transmission End	TEND	Not possible

5. ROM

fig19.2 Flash Memory State Transitions

【Before】

Reset state ⟶ Boot mode

MD1=0,MD2=1,FEW=1

【After】

Reset state ⟶ Boot mode

MD1=1,MD2=0,FEW=1

Table 19.2 Pin Configuration

【Before】

TxD0 Output Serial transmit data output

RxD0 Input Serial receive data input

【After】

TxD1	Output	Serial transmit data output
RxD1	Input	Serial receive data input

6. Power-Down Modes

Low-Power Control Register (LPWRCR)

【Before】

Bit Name	Initial Value	R/W
STS2	0	R/W
STS1	0	R/W
STS0	0	R/W

【After】

STS2	1	R/W
STS1	0	R/W
STS0	1	R/W