To our customers,

# Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Jul.11.2005

# RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

| Product Category | MPU&MCU | | Document No. | TN-H8*-A309A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | H8/38086R Group, H8/38076R Group, H8/38602R Group<br>Watchdog Timer Usage note. | | Information Category | Technical Notification | | |
| Applicable Product | H8/38086R Group<br>H8/38076R Group<br>H8/38602R Group | Lot No.<br>All | Reference Document | H8/38086 Hardware Manual<br>(REJ09B0182-0200 Rev2.00)<br>H8/38076 Hardware Manual<br>(REJ09B0093-0300 Rev3.00)<br>H8/38602 hardware manual<br>(REJ09B0152-0200 Rev2.00) | | |

We would like to inform you about H8/38086R Group,H8/38076R Group and H8/38602R Group Watchdog Timer Usage note.

H8/38086R Group Hardware Manual (Page 306)

H8/38076R Group Hardware Manual (Page 304)

14.5.3 The method of cleaning WT/$\overline{IT}$ bit or IWOVF bit in TCSRWD2 to 0

H8/38602R Group Hardware Manual (Page 208)

12.5.3 The method of cleaning WT/$\overline{IT}$ bit or IWOVF bit in TCSRWD2 to 0

Added
…watchdog timer enters module standby mode.

1x.5.3 The method of clearing WT/$\overline{IT}$ bit or IEOVF bit in TCSRWD2 to 0

When you clear WT/$\overline{IT}$ bit or IEOVF bit in timer control/status register WD2 (TCSRWD2) to 0, you may fail to clear these bit to 0 depending on the program address. In particular, if low two bits of the address of the MOV.B instruction to transfer a value to TCSRWD2 are "10", WT/$\overline{IT}$ bit or IEOVF bit are cleared to0. But if low two bits of the address are "00", WT/$\overline{IT}$ bit or IEOVF bit are not cleared to 0. To avoid this failure, you must use the assembly program shown in fig.12.5 when you clear WT/$\overline{IT}$ bit or IEOVF bit to 0. You must specify TCSRWD2 in 8-bit absolute address, and specify LABEL in 16-bit absolute address. Don't change instructions or add new instructions. The value of "xx" in line 1 and line 4 must be set as shown in fig.12.6. Rn and Rm must use an arbitrary 8-bit general register. And "Address1" in figure.12.5 shows an example that WT/$\overline{IT}$ bit or IEOVF bit are cleared to 0 successfully by the MOV.B instruction in line 2. "Address2" shows an example that WT/$\overline{IT}$ bit or IEOVF bit are not cleared to 0 by the MOV.B instruction in line 2 and cleared to 0 by the MOV.B instruction in line 6.

```
Address1  Address2  Assembly program
H'00A0    H'0232            MOV.B   #H'xx,Rn
H'00A2    H'0234            MOV.B   Rn,@TCSRWD2:8  ; Clear success in case of Address1 and
                                                   ;  failure in case of Address2
H'00A4    H'0236            MOV.B   @TCSRWD2:8,Rm  ; TCSRWD2 read
H'00A6    H'0238            AND.B   #H'xx,Rm       ; Judgment of clear
H'00A8    H'023A            BEQ     LABEL:16       ; Jumps to LABEL if it is a clear success
H'00AC    H'023E            MOV.B   Rn,@TCSRWD2:8  ; Clear success in case of Address2
H'00AE    H'0240  LABEL:    NOP
```

Figure.12.5 The assembly program for clearing WT/$\overline{IT}$ bit or IEOVF bit to 0

| Bit(s) cleared to 0 | The value of "xx" in line 1 | The value of "xx" in line 4 |
|---|---|---|
| Both WT/$\overline{IT}$ and IEOVF | 07 | 28 |
| Only WT/$\overline{IT}$ | 17 | 20 |
| Only IEOVF | 47 | 08 |

Figure.12.6 The value of "xx"