To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Mar.25.2004

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-267A/EA	Rev.	1.0
Title	H8/36912 Group and H8/36902 Group specification changes		Information Category	Specification change		
Applicable Product	H8/36912 Group and H8/36902 Group	Lot No. All	Reference Document	H8/36912 Group, H8/36902 Group Hardware Manual REJ09B0105–0100Z Rev.1.0		

We wish to notify you of the following changes in H8/36912 Group and H8/36902 Group single–chip microcomputers, as detailed below.

1. Changes are shown below.

Section5 Clock Pulse Generators

[Before change]

Backup of the external oscillation halt is available.

[After change]

Backup of the external oscillation halt is not available.

2. Changes in H8/36912 Group and H8/36902 Group Hardware Manual are shown below.

<table>
<tr><th>Item</th><th>Page</th><th>Revisions (See Manual for Details)</th></tr>
<tr><td>Section 5 Clock Pulse Generators
5.1 Features
Backup of the external oscillation halt</td><td>66</td><td>Item deleted
This system detects the external oscillation halt. If detected, the system clock source is automatically switched to the internal RC oscillation clock.</td></tr>
<tr><td>5.2.4 Clock Control/Status Register (CKCSR)</td><td>70</td><td>[Before change]
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>5</td><td>OSCBAKE</td><td>0</td><td>R/W</td><td>External Clock Backup Enable
0: External clock backup disabled
1: External clock backup enabled
The detection circuit for the external clock is enabled when this bit is 1. When the external clock halt is detected while this LSI operates on the external clock, the system clock source is automatically switched to the internal RC oscillator regardless of the value of bit 4 in this register.
Usage Note: The detection circuit for the external clock operates on the internal RC clock. When this bit is set to 1, do not set the internal RC oscillator to the standby state by the RCSTP bit in RCCR.</td></tr>
</table>
[After change]
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>5</td><td>—</td><td>0</td><td>R/W</td><td>Reserved
Although this bit is readable/writable, it should not be set to 1.</td></tr>
</table></td></tr>
</table>

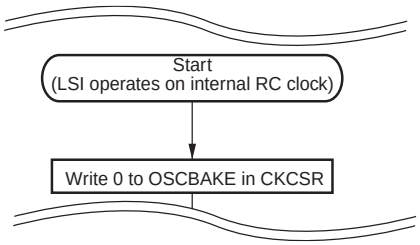
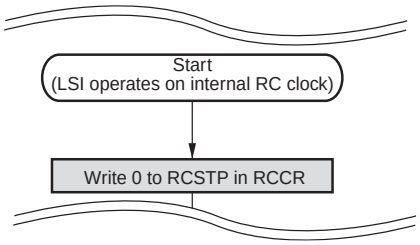
Item	Page	Revisions (See Manual for Details)
5.2.4 Clock Control/Status Register (CKCSR)	70	[Before change]

Bit	Bit Name	Initial Value	R/W	Description
4	OSCSEL	0	R/W	LSI Operation Clock Select • When OSCBAKE = 0 This bit forcibly selects the system clock of this LSI. 0: Selects the internal RC clock as the system clock. 1: Selects the external clock as the system clock. • When OSCBAKE = 1 This bit switches the internal RC clock to the external clock. When this LSI operates on the internal RC clock, setting this bit to 1 switches the system clock to the external clock. [Setting condition] • When 1 is written to this bit while the CKSWIF bit is 0. [Clearing conditions] • When 0 is written to this bit When the external clock halt is detected while OSCBAKE = 1

[After change]

Bit	Bit Name	Initial Value	R/W	Description
4	OSCSEL	0	R/W	LSI Operation Clock Select This bit selects the system clock of this LSI. 0: Selects the internal RC clock as the system clock. 1: Selects the external clock as the system clock.

Item	Page	Revisions (See Manual for Details)
5.2.4 Clock Control/Status Register (CKCSR)	71	[Before change] **Bit** **Bit Name** **Initial Value** **R/W** **Description** 1 OSCHLT 1 R External Clock Halt Detection Flag • When OSCBAKE = 1 This bit indicates the checking result of the external clock state. 0: External oscillation is in use 1: External oscillation is halted. • When OSCBAKE = 0 This bit is meaningless. This bit is always read as 1. [After change] **Bit** **Bit Name** **Initial Value** **R/W** **Description** 1 — 1 R Reserved This bit is always read as 1.
5.3 System Clock Select Operation Figure 5.2 State Transition of System Clock	71	[Before change] Note : * Conditions for the state transition are as follows : — When the external oscillation halt is detected while the backup function is enabled. — When the external clock is switched to the internal RC clock by user software while the backup function is disabled [After change] Note : *When the external clock is switched to the internal RC clock by user software.
Item	**Page**	**Revisions (See Manual for Details)**
5.3.1 Clock Control Operation	72	[Before change] The LSI system clock is generated by the internal RC clock after a reset. The internal RC clock is switched to the external clock by the user software. Figure 5.3 shows the flowchart to switch clocks with the external oscillator backup function enabled. Figures 5.4 and 5.5 show the flowcharts to switch clocks with the external oscillator backup function disabled. [After change] The LSI system clock is generated by the internal RC clock after a reset. The internal RC clock is switched to the external clock by the user software. Figures 5.4 and 5.5 show the flowcharts to switch clocks.
Figure 5.3 Flowchart of Clock Switching with Backup Function Enabled	72	Figure 5.3 deleted.
Figure 5.4 Flowchart of Clock Switching (1) (From Internal RC Clock to External Clock)	73	Figure title amended.

Item	Page	Revisions (See Manual for Details)
Figure 5.5 Flowchart of Clock Switching (2) (From External Clock to Internal RC Clock)	74	Figure title amended. [Before change]  [After change] 
Figure 5.8 External Oscillation Backup Timing	77	Figure 5.8 deleted.
Section 19 List of Registers 19.2 Register Bits	285	[Before change]

Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1
CKCSR	PMRC1	PMRC0	OSCBAKE	OSCSEL	CKSWIE	CKSWIF	OSCHLT

[After change]

Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1
CKCSR	PMRC1	PMRC0	—	OSCSEL	CKSWIE	CKSWIF	—