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RENESAS TECHNICAL UPDATE

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Product Category	Development Environment		Document No.	TN-EML-A139A/E	Rev.	1.00
Title	H8/36109 group expansion I/O board for the E6000: Problems with the timing of the slave interface		Information Category	Technical Notification		
Applicable Product	H8/36109 group expansion I/O board (model name: HS36109EIO61H)	Lot No. 0001 to 0031, 0BA0001B	Reference Document	H8/36109 group expansion I/O board HS36109EIO61H user's manual (REJ10J1320-0100)		

Thank you for using our products.

We have found three problems with the slave interface in the H8/36109 group expansion I/O board (HS36109EIO61H).

Please read the following report before you use the expansion I/O board.

[Problems]

1. When the target system is using additional functions specific to the H8/36109 group (timer RC, timer RD, SCI3, and A/D converter) and access to a register in any of those modules is attempted, the value of the register may accidentally be rewritten. How often this problem will occur depends on the user program code. This problem has already been corrected in lot 0017 and later.

2. When the target system is using additional functions specific to the H8/36109 group (ports G to J) and access to a register in any of those modules is attempted in subactive mode, incorrect values may be read out. This problem does not occur in active mode.

3. When the H8/36109 E6000 emulator (HS36109EIO61H + HS3664EPI62H or HS3664EPI61H) enters a standby mode, the H8/3664 EV-chip also enters the standby mode but the H8/36109 slave chip does not.

The difference in specification is given below.

Aimed specification: The output level on port registers is Hi-Z (high impedance).

Current specification: The values of port registers prior to entering the standby mode are retained.

This problem occurs only when the HS36109EIO61H is in use.

[H8/36109 E6000 System Configuration]

The actual H8/36109 is a single-chip MCU. Thus the address-bus, data-bus, and strobe signals are connected within the MCU (see figure 1).

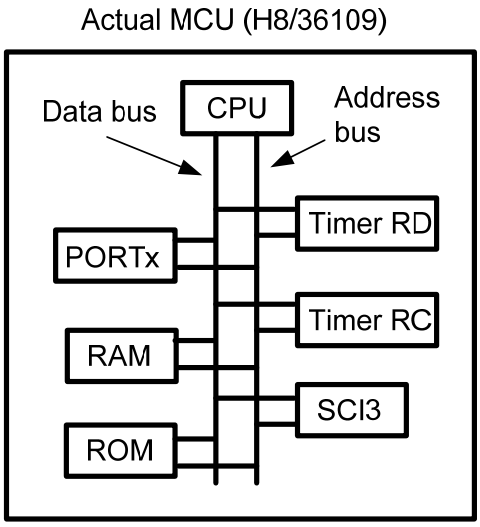

Figure 1 H8/36109's Block Diagram

The E6000 emulator, on the other hand, uses the H8/36109 in emulator mode*. For emulation, an EV chip is used in conjunction with the H8/36109 in emulator mode (hereafter referred to as the slave chip) (see figure 2). For this reason, address-bus, data-bus, and strobe signals are supplied from the EV chip to the slave chip.

*When the H8/36109 MCU is in emulator mode (i.e. not in user mode), the external device (H8/3664 EV chip) supplies the address-bus signal to the MCU.

Figure 2 shows a block diagram of the E6000 system including the H8/36109 MCU.

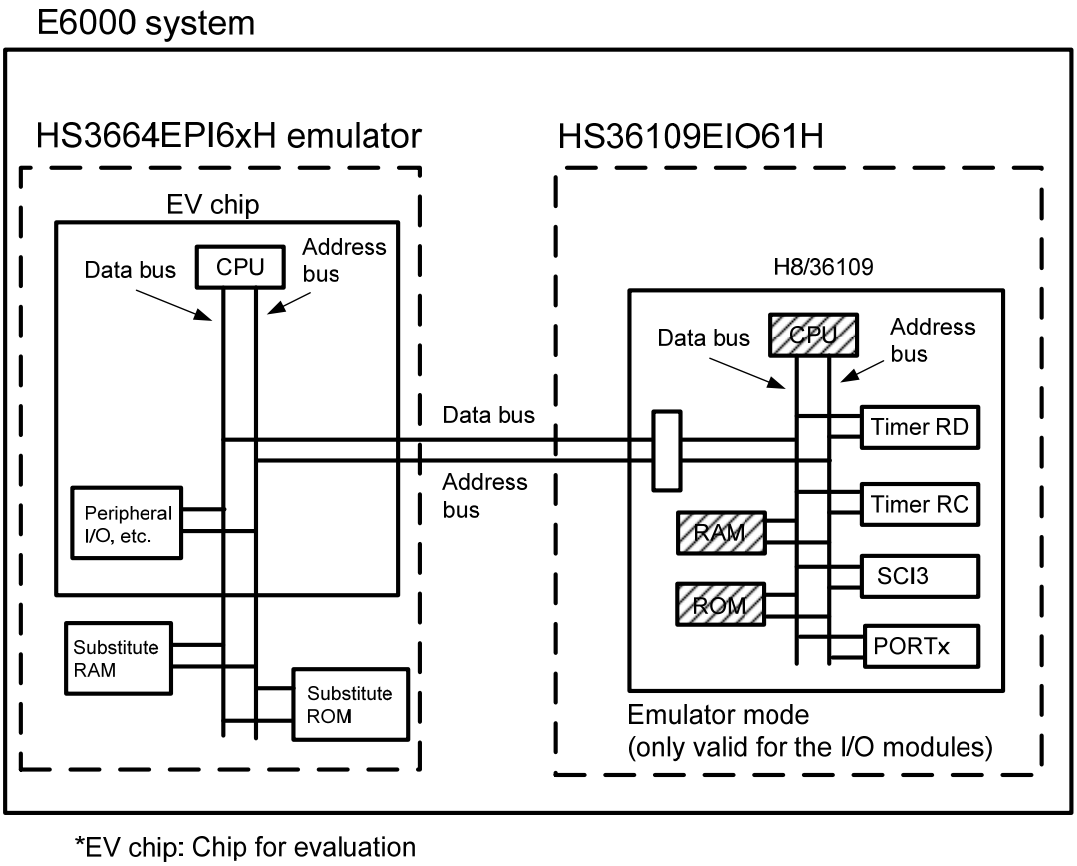

Figure 2 Block Diagram of the E6000 System

[Causes]

1. This problem occurs only when the H8/36109 is used in emulator mode. The address-bus timing within the slave chip was earlier than the timing of other signals (data-bus and select signals) and this led to insufficient holding time between the slave address and select signals.
When the H8/36109 is used alone, however, this problem does not occur because of the difference in configuration as shown in the figures.
2. This problem occurs only when the H8/36109 is used in emulator mode. The timing of negating the slave-chip read signal (which is input from the EV chip to the slave chip) was earlier than the internal clock timing. So the data-bus signal output from the slave chip was negated a half clock cycle earlier and the EV chip could not read the correct value.
When the H8/36109 is used alone, however, this problem does not occur because of the difference in configuration as shown in the figures.
3. The standby control signal was not connected between the H8/3664 E6000 emulator (HS3664EPI62H) and H8/36109 expansion I/O board (HS36109EIO61H).
This problem occurs only when the HS36109EIO61H is in use.

[Resolutions]

Please contact your local distributor if you are using the HS36109EIO61H. Upon your request, we will repair the HS36109EIO61H and HS3664EPI62H. Repairs are necessary only when the HS3664EPI62H is used in conjunction with the HS36109EIO61H.

1. We will delay the timing of an input to the pins of the slave chip by approximately a half cycle (e.g. 25 ns in operation at 20 MHz), considering the delay time within the slave chip.
2. We will adjust the timing, considering the delay time within the slave chip, so that the ASESLRDN signal input to the slave chip will be negated following the falling edge of the T4 cycle with a delay in accord with the AC characteristics of the slave chip.
3. We will add a standby control register to the FPGA logic installed in the H8/3664 E6000 emulator (HS3664EPI62H).
*Note that this modification does not apply to the HS3664EPI61H.
We will also modify the H8/3664 E6000 emulator software (HS3664EPI62SR) so that the standby control register will be enabled when the H8/36109 is selected.

All products for which these problems have been corrected will be labeled “Slave interface corrected”.