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HITACHI MICROCOMPUTER TECHNICAL UPDATE

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THEME	Guide concerning CKIO wiring design of SH-4		
CLASSIFICATION	☐ Spec change ☐ Limitation on Use ■ Supplement of Documents		
PRODUCTNAME	SH7750 SH7750S SH7751	Lot No.etc.	All
REFERENCE DOCUMENTS	SH7750 series Hardware Manual (Rev.1 - 5) SH7751 Hardware Manual (Rev.1 - 2)	Rev. -	EffectiveDate Eternity From

Guide concerning CKIO wiring design of SH-4

SH-4(SH7750,SH7750S,SH7751) matches the phase of the chip internal clock Bö and external clock CKIO signal by feeding back the CKIO output signal to internal PLL circuit 2, and enables high-speed external bus operation. However, PLL lock comes off when the glitch distortion of originating like the reflection noise etc. is generated in the vicinity of the CKIO pin, it is to become causes the system malfunction occasionally. The guide when the board which uses SH-4 is designed in this material is shown.

1. Design and verification of board which uses IBIS

The design result is recommended to be verified by using the IBIS simulation when the board is designed by using SH-4.
The design verification procedure which uses the IBIS simulation is shown below.

1) The IBIS model of all devices with which SH-4 and the CKIO signal of SH-4 are connected is prepared.
2) The characteristic impedance of the CKIO signal of the board is evaluated
   (Refer to following item#3 “Characteristic impedance evaluation and the IBIS simulation”).
3) IBIS is simulated by using result of above mentioned 1) and 2), then result is judged.
   (Refer to following item #2 “Judgment method”).

The error must be included in the characteristic impedance evaluation of the substrate, and consider this error as a margin, in addition, confirm the waveform by real machine in the judgment.

2. Judgment method

Figure 1 shows the method of judgement of the IBIS simulation result.

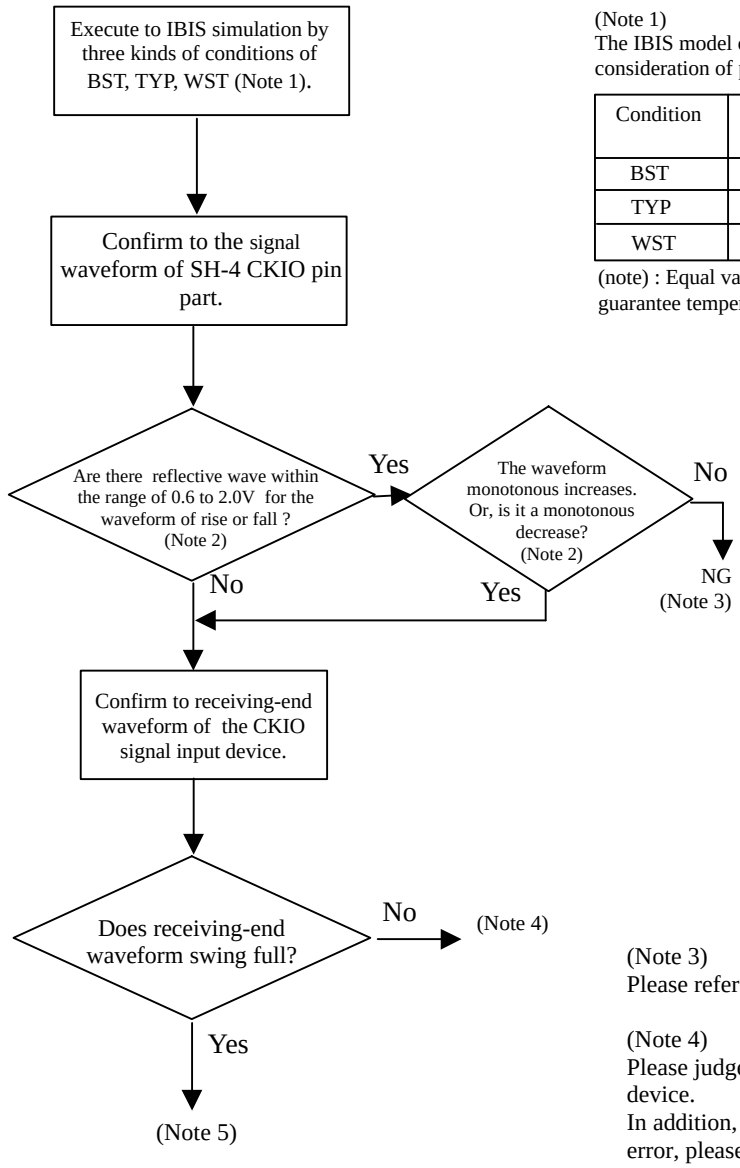


Figure 1 : Judgment flow of IBIS simulation result

(Note 1)

The IBIS model of SH-4 can be selected following three conditions, in consideration of power-supply voltage, temperature, and device disunited.

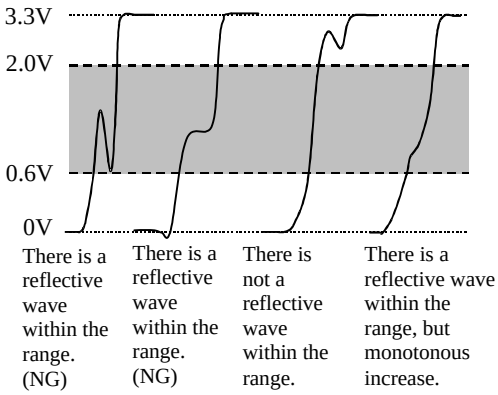
Condition	Power-supply voltage (Vddq)	Temperature(Tj)	Device
BST	3.6V	-20/-40ºC(note)	High speed
TYP	3.3V	25ºC	Standard
WST	3.0V	125ºC	Low speed

(note) : Equal value as the lower limit value of the product in the operation guarantee temperature Ta.

(Note 2)

The example of the waveform is shown in below chart.

During the fixed time, reflected wave of becoming fixed voltage can become glitch inside SH-4.



(Note 3)

Please refer to the following [Supplement].

(Note 4)

Please judge based on the specification of the receiving-edge side device.

In addition, after considering the substrate impedance evaluation error, please confirm the final judgement used by real machine .

(Note 5)

After considering the substrate impedance evaluation error, please confirm final judgement used by real machine.

3. Characteristic impedance evaluation and IBIS simulation

The characteristic impedance of the board can be evaluated with a transmission route simulator (the Interconnectix made by MentorGraphics, the XTK made by Innoveda , , etc. for instance)

Moreover, it is also possible to receive the design support of the board equipped with SH-4 from Zuken Inc. as a method of raising the level of the evaluation.

Zuken Inc. is simulating the characteristic impedance extraction and IBIS of the board with a transmission route simulator.

When you evaluate the characteristic impedance without using these tools on the desk, please design with to secure enough margin.

[Supplement] Principle of glitch generation cause and measures

The outline chart when one SDRAM is connected with the CKIO part is shown in Figure 2 (Package model and substrate wiring from PIN to Rd are omitted).

The impedance of the output buffer is r, the series termination resistance is Rd, the characteristic impedance of substrate wiring is Z0.

In A point is the pin of SH-4, in B point is pin of SDRAM.

The signal waveform output from SH-4 reflects in B point.

When the condition of "Rd=0 and r=Z0", the reflected wave is generated in the voltage of almost 0.5* Vddq in A point.

The reflected wave is more or less generated as long as a complete impedance match is not achieved.

The transmission route as actually separates, and is as the branch complex as Figure 2 as the output impedance of the output buffer changes depending on the output level, too though can define potential Var and Vaf where the reflected wave is generated.

The method of suppressing the reflected wave which adjusts each parameter as shown in Table 1, and moving the potential of the reflected wave outside the VLT(logical threshold voltage : at SH-4, it is from V_{IL}(max) to V_{IH}(min).) range in the input buffer is effective as measures.

It is difficult to obtain the waveform of the reflected wave in an actual board by using an analytical expression, therefore strongly recommends confirming by the simulation.

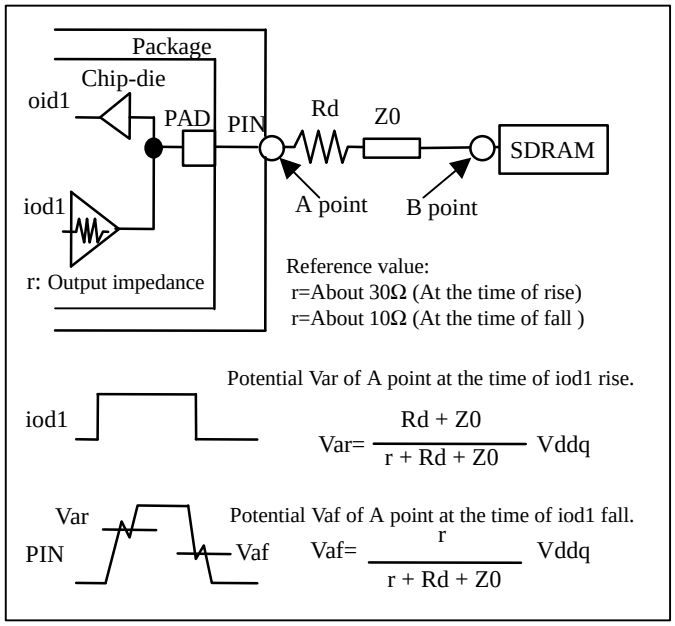


Figure 2 : Rough estimate of glitch generation potential

Table 1: Parameter and contents for adjustment

Parameter	Contents
Rd	The influence of the reflected wave is eased, and moves outside the VLT range in the input buffer. The signal amplitude in the receiving-end device does not swing full in the worst condition occasionally.
Z0	There is a physical restriction within the range where impedance can control.
Receiving-end capacity "At Figure2 SDRAM"	The number and the capacity of the device which receives the clock are adjusted, relates to the influence of the reflected wave caused in sending-end.

[Reflection on transmission route]

From the above, explained the reflection from the receiving-end, even if the characteristic impedance of wiring is not an adjustment, the reflection is generated. Here, explains this content.

The line is terminated at impedance Zb like Figure 3, and the voltage spreads to the line as a traveling wave when the step voltage of amplitude E is impressed to the transmission route of length *l* through impedance r.

All electric powers are not able to be absorbed by the terminal impedance when reaches B point, and reflect at a part.

The voltage which can be reflected by reflection coefficient r_b of B point progresses toward A point.

In A point, reflects by reflection coefficient r_a of A point, and progresses to B point again.

Voltage VA of A point is shown by the expression (1) as a result by repeat this.

$$VA = \frac{Zo}{r + Zb} E \frac{e^{\gamma\lambda} + r_b e^{-\gamma\lambda}}{e^{\gamma\lambda} - r_a r_b e^{-\gamma\lambda}} \qquad (1)$$

$$\left(r_a = \frac{r - Zo}{r + Zo} \quad r_b = \frac{Zb - Zo}{Zb + Zo} \right)$$

$\gamma = \alpha + s/vp$

γ :Attenuation constant of line

vp :Propagation constant of line

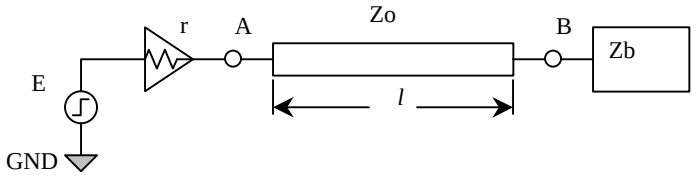


Figure 3 : The line of length *l* by which impedance is connected with sending-end and receiving-end

From these expressions, the signal which can be reflected with B point is superimposed to A point in the delay of *l*/*vp* while attenuating, therefore, the difference and the distortion will be caused in the waveform of A point.

To reduce a waveform warp of A point by the reflection, the following method is devised.

(1)To reduce the reflection with B point, brings close to Zo=Zb.

→ Impedance Zb optimization.

(2) The attenuation constant of the line is enlarged, and the reflected wave is attenuated.

→ Resistance Rd is inserted in the series on the line.

"Refer to Figure 2. However, if resistance Rd is too enlarge, waveform with B point becomes dull, and the amplitude becomes decrease.

When the clock wiring is actual, it is not a simple transmission route like Figure 3, to diverge like Figure 4, and the output impedance in the signal source may change for CMOS depending on the amplitude, to become very complex.

Therefore, it is difficult to obtain the waveform with A point by using an analytical expression.

Then, it is necessary to verify the distortion of waveform by the simulation.

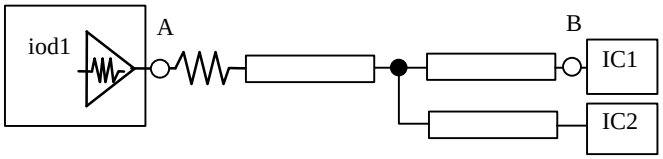


Figure 4 : Transmission line with branch