Date: Jan. 7, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A0072A/E	Rev.	1.00
Title	GPT : Modified description for OADF and OBDF bits		Information Category	Technical Notification		
Applicable Product	The following product groups S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2	Lot No. All	Reference Document	The following User's Manual S124 Rev.1.30, S128 Rev.1.10, S1JA Rev.1.40, S3A1 Rev.1.20, S3A3 Rev.1.10, S3A6 Rev.1.20, S3A7 Rev.1.40, S5D3 Rev.1.10, S5D5 Rev.1.30, S5D9 Rev.1.30, S7G2 Rev.1.40		

Description for the OADF and OBDF bits changed to avoid confusion with OAE and OBE bits.

Blue colored characters indicate a changed part.

[Current description]

Bit	Symbol	Bit name	Description	R/W
b8	OAE	GTIOCA Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b10,b9	OADF[1:0]	GTIOCA Pin Disable Value Setting	b10 b9 0 0: Output disable is prohibited 0 1: GTIOCA pin is set to Hi-Z on output disable 1 0: Set GTIOCA pin to 0 on output disable 1 1: Set GTIOCA pin to 1 on output disable.	R/W
b24	OBE	GTIOCB Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b26,b25	OBDF[1:0]	GTIOCB Pin Disable Value Setting	b26 b25 0 0: Output disable is prohibited 0 1: GTIOCB pin is set to Hi-Z on output disable 1 0: GTIOCB pin is set to 0 on output disable 1 1: GTIOCB pin is set to 1 on output disable.	R/W

OAE bit (GTIOCA Pin Output Enable)

The OAE bit disables or enables the GTIOCA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of GTIOCA pin when an output disable request occurs.

OBE bit (GTIOCB Pin Output Enable)

The OBE bit disables or enables the GTIOCB pin output.

When GTCCRB register is used as the input capture register (at least one bit in GTICBSR register is set to 1), the GTIOCB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of GTIOCB pin when an output disable request occurs.

[Changed description]

Bit	Symbol	Bit name	Description	R/W
b8	OAE	GTIOCA Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b10,b9	OADF[1:0]	GTIOCA Pin Disable Value Setting	b10 b9 0 0: None of the below options are specified 0 1: GTIOCA pin is set to Hi-Z in response to control the output negation 1 0: Set GTIOCA pin to 0 in response to control the output negation 1 1: Set GTIOCA pin to 1 in response to control the output negation.	R/W
b24	OBE	GTIOCB Pin Output Enable	0: Output is disabled 1: Output is enabled.	R/W
b26,b25	OBDF[1:0]	GTIOCB Pin Disable Value Setting	b26 b25 0 0: None of the below options are specified 0 1: GTIOCB pin is set to Hi-Z in response to control the output negation 1 0: GTIOCB pin is set to 0 in response to control the output negation 1 1: GTIOCB pin is set to 1 in response to control the output negation.	R/W

OAE bit (GTIOCA Pin Output Enable)

The OAE bit disables or enables the GTIOCA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of GTIOCA pin in response to a request to disable output from the POEG.

OBE bit (GTIOCB Pin Output Enable)

The OBE bit disables or enables the GTIOCB pin output.

When GTCCRB register is used as the input capture register (at least one bit in GTICBSR register is set to 1), the GTIOCB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of GTIOCB pin in response to a request to disable output from the POEG.

[Changed section for each applicable product]

S124 : 19.2.14 General PWM Timer I/O Control Register (GTIOR)

S128 : 20.2.14 General PWM Timer I/O Control Register (GTIOR)

S1JA : 21.2.14 General PWM Timer I/O Control Register (GTIOR)

S3A1 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

S3A3 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

S3A6 : 22.2.14 General PWM Timer I/O Control Register (GTIOR)

S3A7 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

S5D3 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

S5D5 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

S5D9 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)

S7G2 : 23.2.14 General PWM Timer I/O Control Register (GTIOR)