

RENESAS TECHNICAL UPDATE

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Product classification	MPU & MCU	Document No.	TN-V85-A010A/E	Rev.	1.00
Title	Further notes about the function of timer/event counter register		Notification classification	Technical Information	
Affected Products	In the main part	Affected production lot	Related documents	User's Manual : Hardware of affected products	
		All lots			

For the V850 series microcontrollers on 2.Affected Products, The following further notes about the function of timer/event counter register is released. In addition, please confirm User's Manual : Hardware of affected products about function of timer/event counter register.

- (1) TMPn counter read buffer register (TPnCNT)
- (2) TMQn counter read buffer register (TQnCNT)
- (3) TAAAn counter read buffer register (TAAAnCNT)
- (4) TABn counter read buffer register (TABnCNT)
- (5) TMTn counter read buffer register (TTnCNT)

1. Notification

- (1) TMPn counter read buffer register (TPnCNT)

If TPnCNT register is read when the TPnCE bit = 0, 0000H is read.

If TPnCNT register is read when the TPnCE bit = 1, the count value of the 16-bit timer can be read.

The count value of the 16-bit counter is different by operation mode as follows.

- External event count mode

The 16-bit counter is set to 0000H at the timing when the TPnCE bit changes from 0 to 1.

After that, the counter counts up from 0001H to 0002H, 0003H, and so on, each time a valid edge of an external event count input is detected.

- Other modes

The 16-bit counter starts counting from the default value FFFFH.

It counts up from FFFFH to 0000H, 0001H, 0002H, 0003H, and so on.

(2) TMQn counter read buffer register (TQnCNT)

If TQnCNT register is read when the TQnCE bit = 0, 0000H is read.

If TQnCNT register is read when the TQnCE bit = 1, the count value of the 16-bit timer can be read.

The count value of the 16-bit counter is different by operation mode as follows.

• External event count mode

The 16-bit counter is set to 0000H at the timing when the TQnCE bit changes from 0 to 1.

After that, the counter counts up from 0001H to 0002H, 0003H, and so on, each time a valid edge of an external event count input is detected.

• Other modes

The 16-bit counter starts counting from the default value FFFFH.

It counts up from FFFFH to 0000H, 0001H, 0002H, 0003H, and so on.

(3) TAAAn counter read buffer register (TAAAnCNT)

If TAAAnCNT register is read when the TAAAnCE bit = 0, 0000H is read.

If TAAAnCNT register is read when the TAAAnCE bit = 1, the count value of the 16-bit timer can be read.

The count value of the 16-bit counter is different by operation mode as follows.

• External event count mode

The 16-bit counter is set to 0000H at the timing when the TAAAnCE bit changes from 0 to 1.

After that, the counter counts up from 0001H to 0002H, 0003H, and so on, each time a valid edge of an external event count input is detected.

• Other modes

The 16-bit counter starts counting from the default value FFFFH.

It counts up from FFFFH to 0000H, 0001H, 0002H, 0003H, and so on.

(4) TABn counter read buffer register (TABnCNT)

If TABnCNT register is read when the TABnCE bit = 0, 0000H is read.

If TABnCNT register is read when the TABnCE bit = 1, the count value of the 16-bit timer can be read.

The count value of the 16-bit counter is different by operation mode as follows.

• External event count mode

The 16-bit counter is set to 0000H at the timing when the TABnCE bit changes from 0 to 1.

After that, the counter counts up from 0001H to 0002H, 0003H, and so on, each time a valid edge of an external event count input is detected.

• Other modes

The 16-bit counter starts counting from the default value FFFFH.

It counts up from FFFFH to 0000H, 0001H, 0002H, 0003H, and so on.

(5) TMTn counter read buffer register (TTnCNT)

If TTnCNT register is read when the TTmECC bit = 0 and the TTmCE bit = 0, 0000H is read.

If TTnCNT register is read when the TTmECC bit = 1 and the TTmCE bit = 0, the previous value is read.

If TTnCNT register is read when the TTmCE bit = 1, the count value of the 16-bit timer can be read.

The count value of the 16-bit counter is different by operation mode as follows.

• External event count mode

The 16-bit counter is set to 0000H at the timing when the TTmCE bit changes from 0 to 1.

After that, the counter counts up from 0001H to 0002H, 0003H, and so on, each time a valid edge of an external event count input is detected.

• Encoder compare mode

A count operation is controlled by TENCm0 and TENCm1 phases.

The 16-bit counter initial setting is performed by transferring the set value of the TTmTCW register to the 16-bit counter and the count operation is started. (When the TTmCTL2.TTmECC bit = 0, the TTmTCW register set value is transferred to the 16-bit counter at the timing when the TTmCTL0.TTmCE bit changes from 0 to 1.)

• Triangular-wave PWM mode

The 16-bit counter starts counting from the initial value FFFFH.

It counts up FFFFH, 0000H, 0001H, 0002H, 0003H, and so on.

Following the count-up operation, the counter counts down upon a match between the 16-bit count value and the CCR0 buffer register.

• Mode other than above

The 16-bit counter starts counting from the initial value FFFFH.

It counts up FFFFH, 0000H, 0001H, 0002H, 0003H, and so on.

2. Affected Products

Products series			
V850ES/FG2	V850ES/FE2	V850ES/FF2	V850ES/FE3
V850ES/FF3	V850ES/FG3	V850ES/FJ3	V850ES/FJ2
V850ES/FK3	V850ES/FE3-L	V850ES/FF3-L	V850ES/FG3-L
V850ES/FE3-N	V850ES/FF3-N	V850ES/FG3-N	V850ES/FJ3-N
V850ES/FK3-N	V850E/RS1	V850E/PG2	V850E/CG4
V850E/RS2	V850E/CAG4-M	V850E/RG3	V850E/PHJ1
V850E/FK3-H	V850E/PHO3	V850E/PHC3	-