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RENESAS TECHNICAL UPDATE

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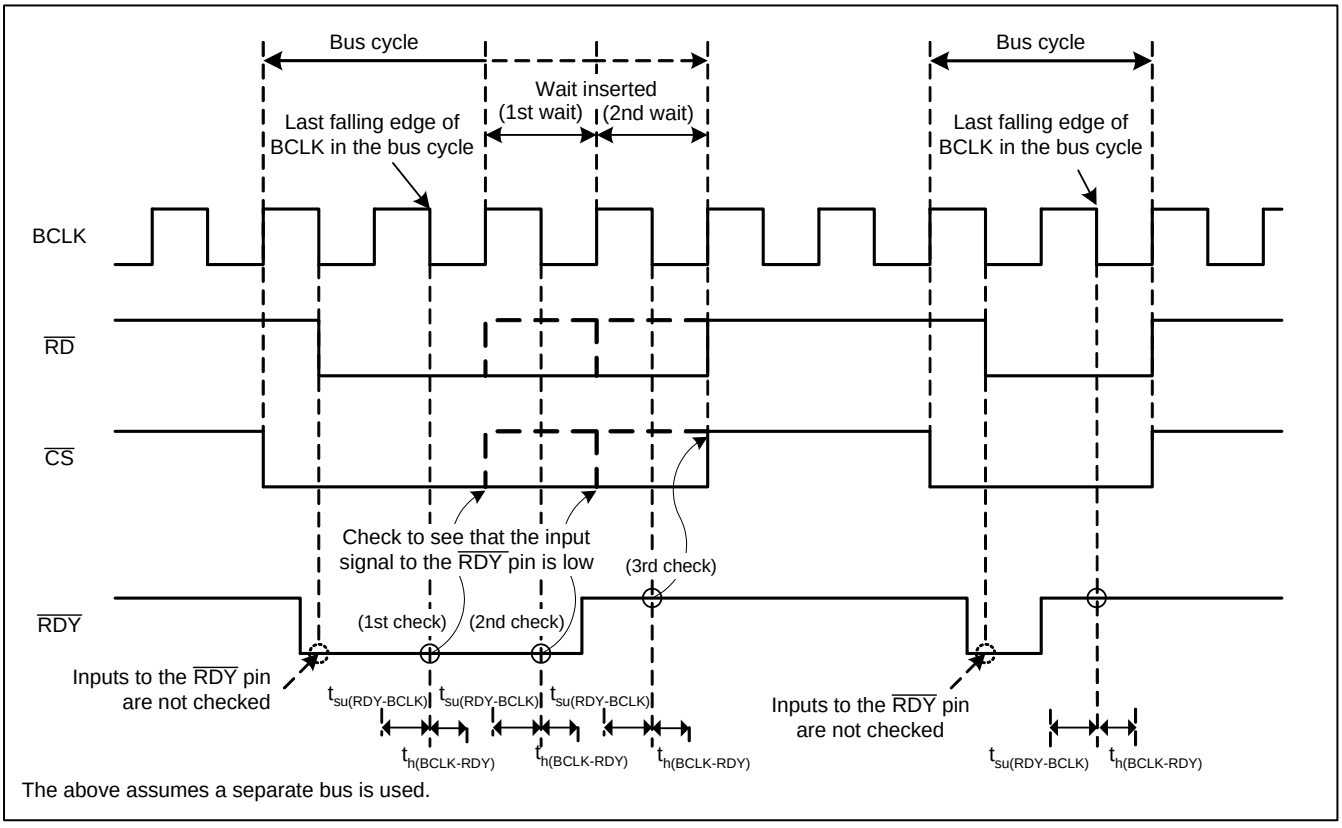
Product Category	MPU & MCU		Document No.	TN-16C-A209A/E	Rev.	1.00
Title	Explanation of the $\overline{\text{RDY}}$ Signal for the M16C/30 Series and M16C/60 Series		Information Category	Technical Notification		
Applicable Products	M16C/30 Series and M16C/60 Series	Lot No. —	Reference Document			

This document explains the bus timing with the $\overline{\text{RDY}}$ signal. Figure 1 shows an Example of Controlling the Bus Timing with the $\overline{\text{RDY}}$ Signal. “One cycle” here indicates one cycle of BCLK.

When a low signal is input to the $\overline{\text{RDY}}$ pin at the last falling edge of BCLK in the bus cycle, a one-cycle wait is inserted (a change of the bus control signal is delayed for one cycle).
After a low signal is detected at the $\overline{\text{RDY}}$ pin, the input signal of the $\overline{\text{RDY}}$ pin is checked at every falling edge of BCLK. When an input signal to the $\overline{\text{RDY}}$ pin is low, a one-cycle wait is inserted; when an input signal is high, a wait is not inserted.
Both high and low inputs to the $\overline{\text{RDY}}$ pin must meet $t_{su(RDY-BCLK)}$ and $t_{h(BCLK-RDY)}$.



The above assumes a separate bus is used.

Figure 1 Example of Controlling the Bus Timing with the $\overline{\text{RDY}}$ Signal