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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A132A/E	Rev.	1.00
Title	Expansion of Specification for Block Erasure of Flash Memory, Disclosure of Specification for FRDYI Interrupt, Addition of Description for Memory Planes, and Correction of Electrical Characteristics for RX100 Series		Information Category	Technical Notification		
Applicable Product	RX110 Group RX111 Group RX113 Group	Lot No. All	Reference Document	RX110 Group User's Manual: Hardware Rev.1.10 (R01UH0421EJ0110) RX111 Group User's Manual: Hardware Rev.1.20 (R01UH0365EJ0120) RX113 Group User's Manual: Hardware Rev.1.02 (R01UH0448EJ0102)		

This document describes the expansion of the specification for block erase, disclosure of the specification for the FRDYI interrupt, and addition of description for memory planes regarding the above applicable products of RX100 series. It also describes the correction of "E2 DataFlash Characteristics" in the Electrical Characteristics section.

- Expansion of the specification for block erase

The area that can be erased by the block erase command will be expanded from "a specified block" to "specified consecutive blocks".

- Disclosure of the specification for the FRDYI interrupt

The following specification of the FRDYI interrupt will be disclosed:
When a software command is executed to the user area, data area, or extra area, an FRDYI interrupt occurs when processing of the executed software command is completed or when the forced stop processing is completed.

- Addition of description for memory planes

When the ROM size exceeds 256 Kbytes, the ROM area is divided into two memory planes on a 256-Kbyte boundary.

Note that this does not apply to the RX110 Group because the ROM sizes in the RX110 Group are less than 256 Kbytes.

- Correction of "E2 DataFlash Characteristics" in the Electrical Characteristics section

Errors in the conditions for the FCLK frequency will be corrected. Note that this does not apply to the RX110 Group because the RX110 Group does not have E2 DataFlash.

The details are described below. Page, section, and table numbers are listed using the RX113 Group as an example in sections below except section 1.2. See the table on the last page for those numbers of the other groups.

1. Expansion of the specification for block erase

1.1 Block erase

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The description for block erase in section 41.4.9 Flash Control Register (FCR) of the Flash Memory section will be changed as follows.

Before change

[Block erase]

- Erase a specified block in the flash memory.

  Set the beginning address of the block to be erased in registers FSARH and FSARL, and the last address in registers FEARH and FEARL. If a value other than the above is set, erasure may not be executed correctly.

After change

[Block erase]

- Erase consecutive areas in the same memory plane in blocks.

  Set the beginning address of the blocks to be erased in registers FSARH and FSARL, and the last address in registers FEARH and FEARL. If a value other than the above is set, erasure may not be executed correctly.

1.2 Block erase time (ROM)

- RX113 Group, RX111 Group (page and section numbers of the RX113 Group are listed)

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Tables 42.61 and 42.62 in section 42.13 ROM (Flash Memory for Code Storage) Characteristics will be changed as follows.

Before change

Table 42.61 ROM (Flash Memory for Code Storage) Characteristics (2) High-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.23	267	—	5.48	214	ms
omitted									

Table 42.62 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.3	269	—	5.85	219	ms
omitted									

After change

Table 42.61 ROM (Flash Memory for Code Storage) Characteristics (2) High-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.23	267	—	5.48	214	ms
	256-Kbyte	t_{BE256K}	—	407	925	—	39	457	ms
omitted									

Table 42.62 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.3	269	—	5.85	219	ms
	256-Kbyte	t_{BE256K}	—	407	928	—	93	520	ms
omitted									

- RX110 Group (page and section numbers of the RX110 Group are listed)

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Tables 32.45 and 32.46 in section 32.8 ROM (Flash Memory for Code Storage) Characteristics will be changed as follows.

Before change

Table 32.45 ROM (Flash Memory for Code Storage) Characteristics (2) High-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.23	267	—	5.48	214	ms
omitted									

Table 32.46 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.3	269	—	5.85	219	ms
omitted									

After change

Table 32.45 ROM (Flash Memory for Code Storage) Characteristics (2) High-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.23	267	—	5.48	214	ms
	128-Kbyte	t_{BE128K}	—	203	463	—	20	228	ms
omitted									

Table 32.46 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	8.3	269	—	5.85	219	ms
	128-Kbyte	t_{BE128K}	—	203	464	—	46	260	ms
omitted									

1.3 Block erase time (E2 DataFlash) and correction of the errors in the Electrical Characteristics section

(This does not apply to the RX110 Group because the RX110 Group does not have E2 DataFlash.)

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Tables 42.64 and 42.65 in section 42.14 E2 DataFlash Characteristics will be changed as follows.

Before change and correction

Table 42.64 E2 DataFlash Characteristics (2): high-speed operating mode

Item		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	17.4	456	—	6.15	228	ms
omitted									

Table 42.65 E2 DataFlash Characteristics (3): middle-speed operating mode

Item		Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	17.5	457	—	7.76	259	ms
omitted									

After change and correction

Table 42.64 E2 DataFlash Characteristics (2): high-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	17.4	456	—	6.15	228	ms
	8-Kbyte	t_{BE8K}	—	60.4	499	—	9.3	231	ms
omitted									

Table 42.65 E2 DataFlash Characteristics (3): middle-speed operating mode

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			min	typ	max	min	typ	max	
omitted									
Erasure time	1-Kbyte	t_{BE1K}	—	17.5	457	—	7.76	259	ms
	8-Kbyte	t_{BE8K}	—	60.5	500	—	16.7	267.6	ms
omitted									

2. Disclosure of the specification for the FRDYI interrupt

2.1 Interrupt vector table

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The interrupt vector table in the ICU section will be changed as follows.

Before change

Table 14.3 Interrupt Vector Table

Source of Interrupt Request Generation	Name	Vector No.	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
omitted										
—	Reserved	23	005Ch	—	×	×	×	—	—	—
omitted										

After change

Table 14.3 Interrupt Vector Table

Source of Interrupt Request Generation	Name	Vector No.	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	sstb Return	IER	IPR	DTCER
omitted										
FCU	FRDYI	23	005Ch	Edge	○	×	×	IER02.IEN7	IPR002	—
omitted										

"○" indicates usability as a CPU interrupt

2.2 Overview

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Table 41.1 will be changed as follows.

Before change

Table 41.1 Flash Memory Specifications

Item	Description
omitted	
Software commands	*omitted*
On-board programming	*omitted*
omitted	

After change

Table 41.1 Flash Memory Specifications

Item	Description
omitted	
Software commands	*omitted*
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	*omitted*
omitted	

2.3 FRDY flag

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The specification of the flash ready flag (FRDY) in section 41.4.20 Flash Status Register 1 (FSTATR1) of the Flash Memory section will be changed as follows.

Before change

FRDY Flag (Flash Ready Flag)

This flag is used to confirm whether a software command is executed.
This flag becomes 1 when processing of the executed software command or the forced stop processing is completed, and this flag becomes 0 when setting the FCR.OPST bit to 0.

After change

FRDY Flag (Flash Ready Flag)

This flag is used to confirm whether a software command is executed.
This flag becomes 1 when processing of the executed software command or the forced stop processing is completed, and this flag becomes 0 when setting the FCR.OPST bit to 0.
Also, an interrupt (FRDYI) is generated when this flag becomes 1.

2.4 EXRDY flag

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The specification of the extra ready flag (EXRDY) in section 41.4.20 Flash Status Register 1 (FSTATR1) of the Flash Memory section will be changed as follows.

Before change

EXRDY Flag (Extra Area Ready Flag)

This flag is used to confirm whether a software command for the extra area is executed.
This flag is set to 1 when processing of the executed software command is completed and 0 when the FEXCR.OPST bit is set to 0.

After change

EXRDY Flag (Extra Area Ready Flag)

This flag is used to confirm whether a software command for the extra area is executed.
This flag is set to 1 when processing of the executed software command is completed and 0 when the FEXCR.OPST bit is set to 0.
Also, an interrupt (FRDYI) is generated when this flag becomes 1.

2.5 Interrupt

The following description will be added to section 41.7 Programming and Erasure of the Flash Memory section.

41.7.5 Interrupt

When software command processing or forced stop processing is completed, an interrupt (FRDYI) is generated.
A software command processing complete interrupt is de-asserted when the FSTATR1.FRDY or FSTATR1.EXRDY flag is set to 0.
Clear the IRn.IR flag before setting the IERm.IEN bit of the ICU corresponding to this interrupt.

3. Addition of description for memory planes

(This does not apply to the RX110 Group because the ROM sizes are less than 256 Kbytes.)

3.1 Memory planes

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The description in section 41.2 ROM Area and Block Configuration and Figure 41.1 will be changed as follows.

Before change

A maximum of 512 Kbytes can be configured in the ROM area. The ROM area is divided into blocks according to the ROM capacity. The ROM area is erased in block units. Figure 41.1 shows the ROM Area and Block Configuration.

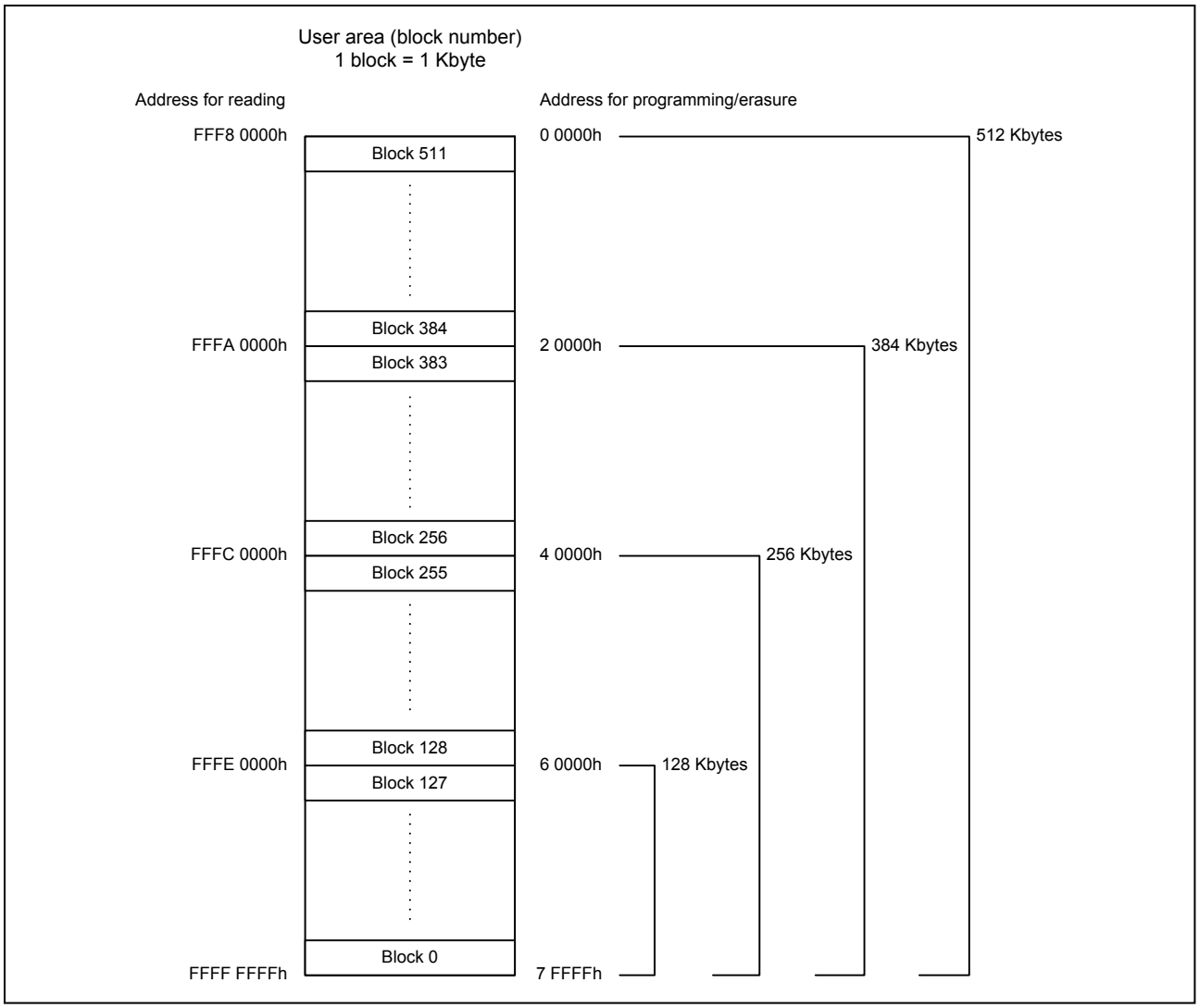

Figure 41.1 ROM Area and Block Configuration

After change

The maximum ROM size of this MCU is 512 Kbytes. Note that when the ROM size exceeds 256 Kbytes, the ROM area is divided into two memory planes on a 256-Kbyte boundary. Each plane is divided into 1-Kbyte areas (blocks), and one plane can have up to 256 blocks. When executing the block erase command, the memory is eased in block units. Figure 41.1 shows the ROM Area and Memory Plane/Block Configuration.

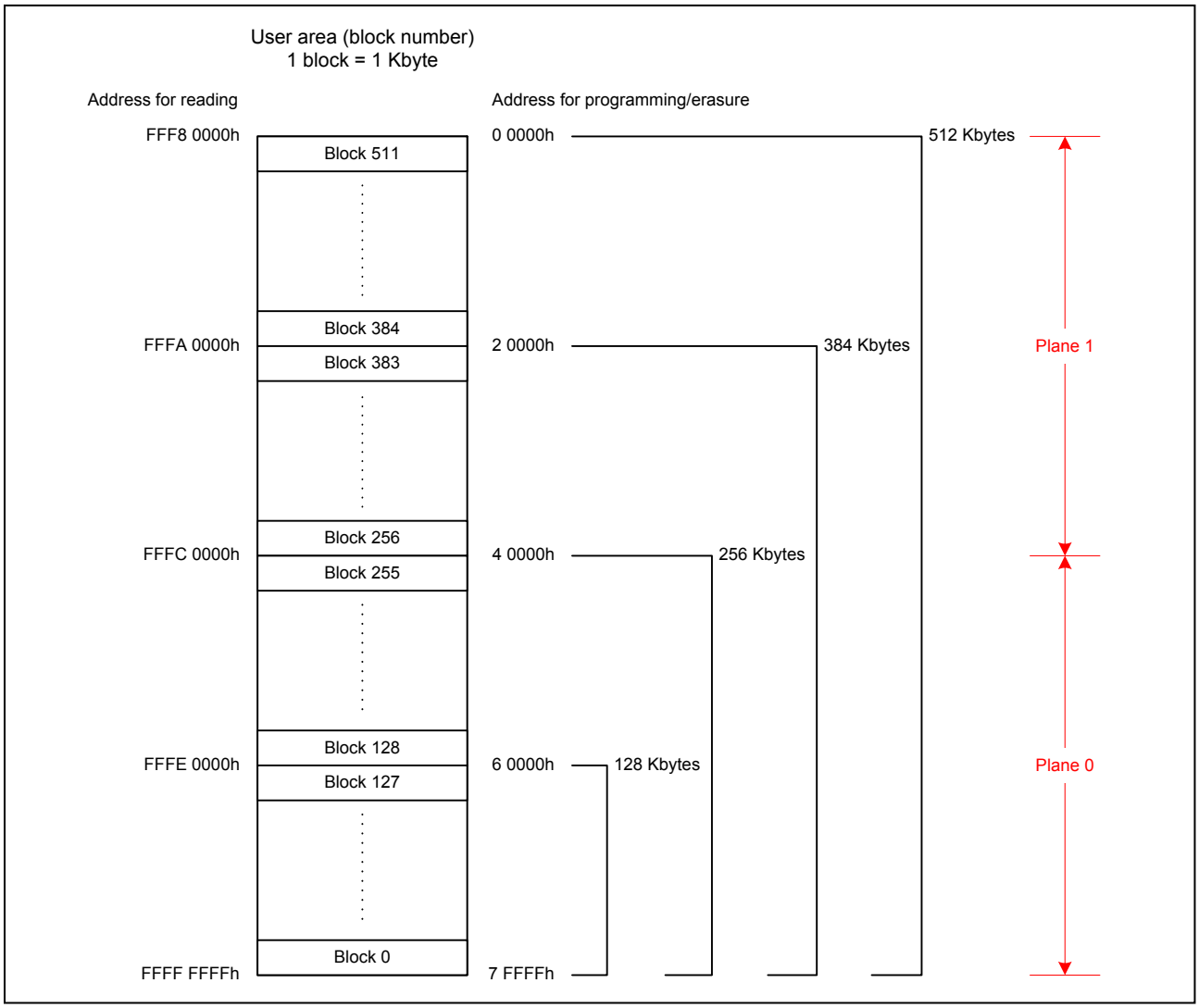

Figure 41.1 ROM Area and Memory Plane/Block Configuration

3.2 Boundary between memory planes (flash control register (FCR))

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The description for products with 384-Kbyte or 512-Kbyte ROM in section 41.4.9 Flash Control Register (FCR) will be changed as follows.

Before change

[Products with 384-Kbyte or 512-Kbyte ROM]

Blank checking cannot be executed across 256-Kbyte boundaries.

After change

[Products with 384-Kbyte or 512-Kbyte ROM]

Blank checking and block erasure cannot span boundaries between memory planes (256-Kbyte boundaries).

3.3 Boundary between memory planes (flash processing end address register L (FEARL))

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The description for products with 384-Kbyte or 512-Kbyte ROM in section 41.4.14 Flash Processing End Address Register L (FEARL) will be changed as follows.

Before change

[Products with 384-Kbyte or 512-Kbyte ROM]

The range specified by registers FSARH and FSARL and registers FEARH and FEARL cannot be set to a range that spans across 256-Kbyte boundaries.

After change

[Products with 384-Kbyte or 512-Kbyte ROM]

Set addresses in the same memory plane for registers FSARH and FSARL and registers FEARH and FEARL.

[Reference]

Section in This Document	Description	Page/Table/Figure Numbers	
		RX110 Group User's Manual: Hardware Rev.1.10	RX111 Group User's Manual Hardware Rev.1.20
1.1	Block erase	Page 849 of 971, 31.3.8	Page 1108 of 1256, 35.4.9
1.2	Block erase time (ROM)	Listed in this document (Page 956 of 971, 32.8, Table 32.45, Table 32.46)	Page 1235 of 1256, 36.10, Table 36.49, Table 36.50
1.3	Block erase time (E2 DataFlash) and correction of the errors in the Electrical Characteristics section	Not applicable because the RX110 Group does not have E2 DataFlash	Page 1236 of 1256, 36.11, Table 36.52, Table 36.53
2.1	Interrupt vector table	Page 235 of 971, Table 14.3	Page 249 of 1256, Table 14.3
2.2	Overview	Page 841 of 971, 31.1, Table 31.1	Page 1097 of 1256, 35.1, Table 35.1
2.3	FRDY flag	Page 857 of 971, 31.3.19	Page 1116 of 1256, 35.4.20
2.4	EXRDY flag	Page 857 of 971, 31.3.19	Page 1116 of 1256, 35.4.20
2.5	Interrupt	Page 872 of 971, 31.6.5	Page 1137 of 1256, 35.7.5
3.1	Memory planes	Not applicable because the ROM sizes are less than 256 Kbytes	Page 1098 of 1256, 35.2, Figure 35.1
3.2	Boundary between memory planes (flash control register (FCR))	Not applicable because the ROM sizes are less than 256 Kbytes	Page 1108 of 1256, 35.4.9
3.3	Boundary between memory planes (flash processing end address register L (FEARL))	Not applicable because the ROM sizes are less than 256 Kbytes	Page 1112 of 1256, 35.4.14